



UNIVERSAL COUNTER

DESCRIPTION

The U_DCNT.VHD ipcore described here is a Universal Counter.

FEATURES

- Up/Down counting
- Modulo counting
- Synchronous and Asynchronous load
- Asynchronous reset
- Rollover indication

VHDL COMPONENT DECLARATION:-

```
COMPONENT U_DCNT
  GENERIC (
    SYN      : INTEGER := 0;
    CNT      : INTEGER := 5;
    FDVD     : INTEGER := 1;
    OBW      : INTEGER := 5
  );
  PORT(
    DIR      : IN  NODE := '0';
    D        : IN  BUS1D(LOG2(OBW) DOWNTO 0) := (OTHERS=>'0');
    LDN      : IN  NODE := '0';
    EC       : IN  NODE := '0';
    CLKI     : IN  NODE := '0';
    RST      : IN  NODE := '1';
    ALDN     : IN  NODE := '1';
    COL      : BUFFER BUS1D(LOG2(OBW)DOWNTO 0) := (OTHERS=>'1');
    EB       : BUFFER NODE;
    COUT     : BUFFER NODE;
    XL       : BUFFER NODE;
    XY       : BUFFER NODE
  );
END COMPONENT;
```

FILES YOU GET

- | | | |
|----------------|---|---|
| i) FUNC.DOC | - | Documentation of functions & data types used in the core. |
| ii) README.DOC | - | Compile and licensing information. |
| iii) UDCNT.DOC | - | This document |
| a) MYLIB.VHD | - | PACKAGE |
| b) U_DCNT.VHD | - | TOP HIERARCHY DESIGN |
| c) M_DFF.VHD | - | FILES USED IN F_IFO |
| d) S_DFF.VHD | - | -do- |
| f) P_AD.VHD | - | -do- |
| g) I_NCDEC.VHD | - | -do- |
| h) A_DSB.VHD | - | -do- |



INPUT PORTS

Port Name	Reqd	Description	Comments
DIR	No	Count direction	1 bit wide, 0 (down count), 1 (up count)
D[log2(CNT)..0]	No	Synchronous load data	log2(CNT)+1 bits wide.
LDN	No	Synchronous load	Active hi, loads D[] to counter. Load will not occur during rollover.
EC	No	Count enable	Active hi, when lo counting is disabled. No effect on load.
CLKI	Yes	Clock	Positive edge triggered clock.
RST	No	Asynchronous reset/load	Active lo. When SYN=0, will load counter with CNT When SYN=1 will reset counter to 0.
ALDN	No	Asynchronous load	Active lo. When SYN=1, will load counter with CNT When SYN=0 not used.

*When SYN=1, the RST and ALDN inputs must not be active together.

OUTPUT PORTS

Port Name	Description	Type	Comments
COL[log2(CNT)..0]	Data output from counter	Registered	WID+1 bits wide
EB	Indicates the following:- Count is zero, when DIR=0 Count is max, when DIR=1	Combinatorial	Anded with the EC input port. Resets counter at rising edge of next CLKI. When SYN=0 count becomes CNT When SYN=1 count becomes all '1'
COUT	Count is zero, when DIR=0 Count is max, when DIR=1	Combinatorial	
XL	1 CLKI after EB	Registered	Hi when RST=lo
XY	1 CLKI after EB	Registered	Lo when RST=lo

PARAMETERS – All parameters are INTEGER type

Parameter	Required	Description
SYN	No	Synchronous(1)/ASYNhronous load(0)
CNT	Yes	When SYN=1, CNT is unused. When SYN=0, CNT is asynchronous load value.
FDVD	No	When FDVD=0, the counter will count an additional count after RST=1 and during rollover, this won't happen when FDVD=1.
OBW	Yes	log2(OBW) is upper index of COL[], D[] ports e.g. LOG2(14)=3. Thus D[3..0], COL[3..0]



SAMPLE DESIGN-(1)

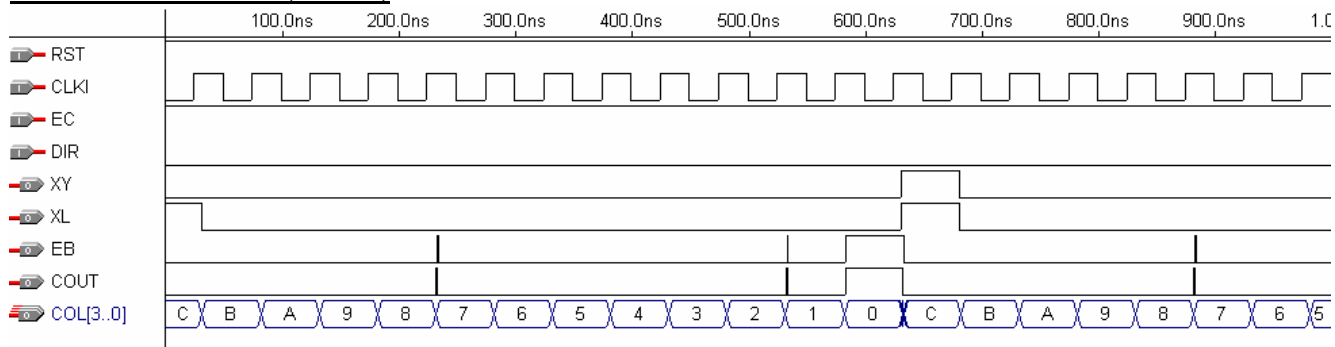
```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
PORT(
    DIR    :IN  NODE;
    D      :IN  BUS1D(LOG2(CNT) DOWNT0 0);
    LDN    :IN  NODE;
    EC     :IN  NODE;
    CLKI   :IN  NODE;
    RST    :IN  NODE;
    COL    :BUFFER BUS1D(LOG2(CNT) DOWNT0 0);
    EB     :BUFFER;
    COUT   :BUFFER;
    XL     :BUFFER;
    XY     :BUFFER
);
END MYTOP;

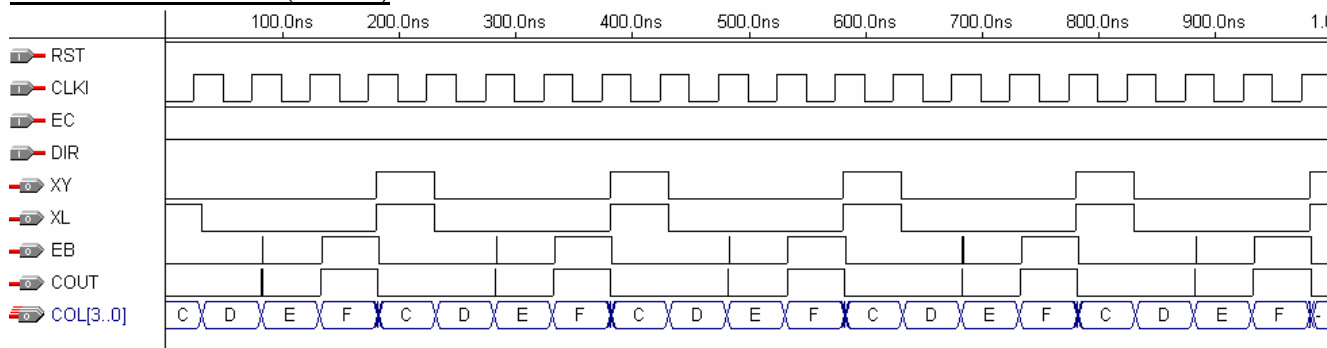
ARCHITECTURE MYTOP OF MYTOP IS
BEGIN
A1: U_DCNT GENERIC MAP (SYN=>0,
    CNT=>12,
    FDVD=>0
    OBW=>12)
    PORT MAP (DIR, D, LDN, EC, CLKI, RST, COL, EB, COUT, XL, XY);
END MYTOP;
```

TIMING DIAGRAM (DIR=0)





TIMING DIAGRAM (DIR=1)



SAMPLE DESIGN-(2)

ARCHITECTURE MYTOP OF MYTOP IS

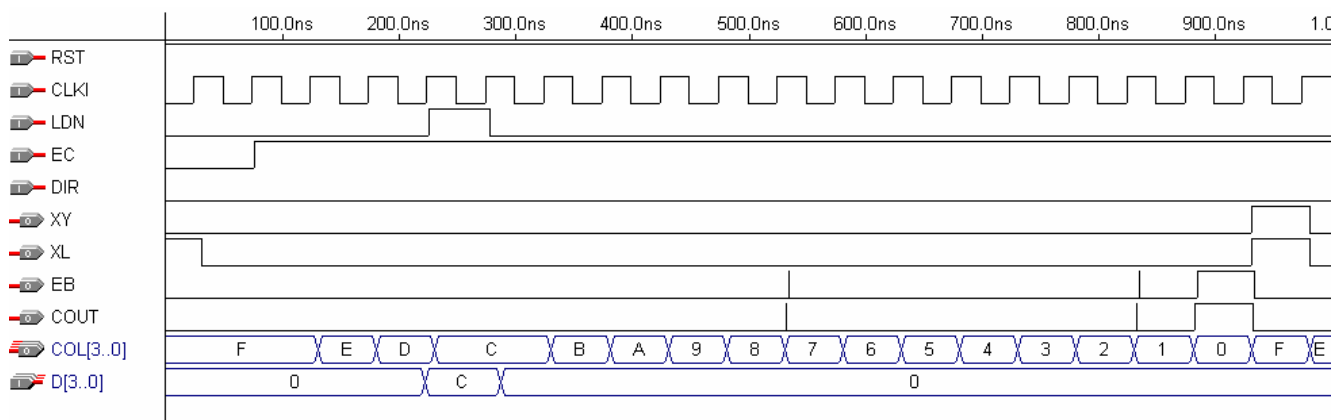
BEGIN

```
A1: U_DCNT GENERIC MAP (SYN=>1,  
                        CNT=>12,  
                        FDVD=>0  
                        OBW=>12)
```

```
PORT MAP (DIR, D, LDN, EC, CLKI, RST, COL, EB, COUT, XL, XY);
```

END MYTOP;

TIMING DIAGRAM (DIR=0)



TIMING DIAGRAM (DIR=1)

