

# STATE GENERATOR

## DESCRIPTION

The S\_TATE.VHD ipcore described here is a synchronous state generator. The number of states are user configurable. All the flip-flops share a common clock and asynchronous reset and enable signals.

## VHDL Component Declaration:

```
COMPONENT S_TATE
GENERIC(
    CNT    : INTEGER:=0;
    WDO    : INTEGER:=0
) ;
PORT(
    BEGD   : IN      NODE:= '1';
    BEGE   : IN      NODE:= '1';
    CLKI   : IN      NODE:= '1';
    RST    : IN      NODE:= '1';
    PRN    : IN      NODE:= '1';
    ENB    : IN      NODE:= '1';
    LSTT   : BUFFER  NODE;
    LCLK   : BUFFER  NODE;
    DCOD   : BUFFER  BUS1D(WDO-1 DOWNT0 0);
    SON    : BUFFER  NODE;
) ;
END COMPONENT;
```

## FILES YOU GET

i)FUNC.DOC	-	Documentation of functions & data types used in the core.
ii)README.DOC	-	Compile and licensing information.
iii)MDFP.DOC	-	This document
a)MYLIB.VHD	-	PACKAGE
b)S_TATE.VHD	-	TOP HIERARCHY DESIGN FILE
c)D_ECOD.VHD	-	DESIGN FILE BELOW TOP HIERARCHY
d)M_DFF.VHD	-	-do-
e)S_DFF.VHD	-	-do-
f)U_DCNT.VHD	-	-do-
g)S_JKF.VHD	-	-do-
h)S_TFF.VHD	-	-do-
i)I_NCDEC.VHD	-	-do-
j)A_DSB.VHD	-	-do-
l)F_DIV.VHD	-	-do-

## **DESCRIPTION**

The process start is indicated with the SON o/p going hi 1 CLKI pulse after BEGD & BEGE go Hi and terminates(SON goes lo) after the number of states specified by the CNT parameter are generated. State transitions occur at the rising edge of the clock enable input ENB and the state count appears on the DCOD o/p. The process restarts when the begin inputs are re-asserted.

## **INPUT PORTS-All 1 bit wide**

NAME	DESC	COMMENTS
BEGD	Start	Begin input. Width $\geq$ 1CLKI. When unused, connect hi or leave unconnected.
BEGE	Start Enable	Enable pulse for BEGD. Width=1CLKI. When unused, connect hi or leave unconnected.
CLKI	Clock	Synchronizes all internal operations.
RST	Reset	Resets all internal registers.
PRN	Preset	Presets the SON o/p. When unused, connect hi or leave unconnected.
ENB	Clock Enable	1 CLKI wide pulse. The duration of each state is the time interval between the ENB inputs. In other words the ENB input causes the state to change. When unused, connect hi or leave unconnected.

## **OUTPUT PORTS**

NAME	DESC	WIDTH	COMMENTS
LSTT	Last State	1	Goes Hi when last state CNT-1 is in progress
LCLK	Last Clock	1	1 CLKI wide pulse at end of LSTT. For continuous operation, the LCLK output may be ORed with the BEGD, BEGE inputs.
DCOD	Decoded state	WDO	Decoded state count. WDO $\geq$ CNT
SON	Process On	1	Goes Hi 1 CLKI after BEGD and stays Hi to the end of LCLK, Hi for CNT clocks. Used only when BEGD & BEGE are used. When ENB is used this output is low.
SCNT	State Count	WDL	State count

## **PARAMETERS**

NAME	REQD	TYPE	MIN	DESCRIPTION
CNT	YES	Integer	0	Number of states
WDO	YES	Integer	1	Width of DCOD output port
WDL	YES	Integer	1	Width of SCNT output port

## SAMPLE DESIGN-1

```

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

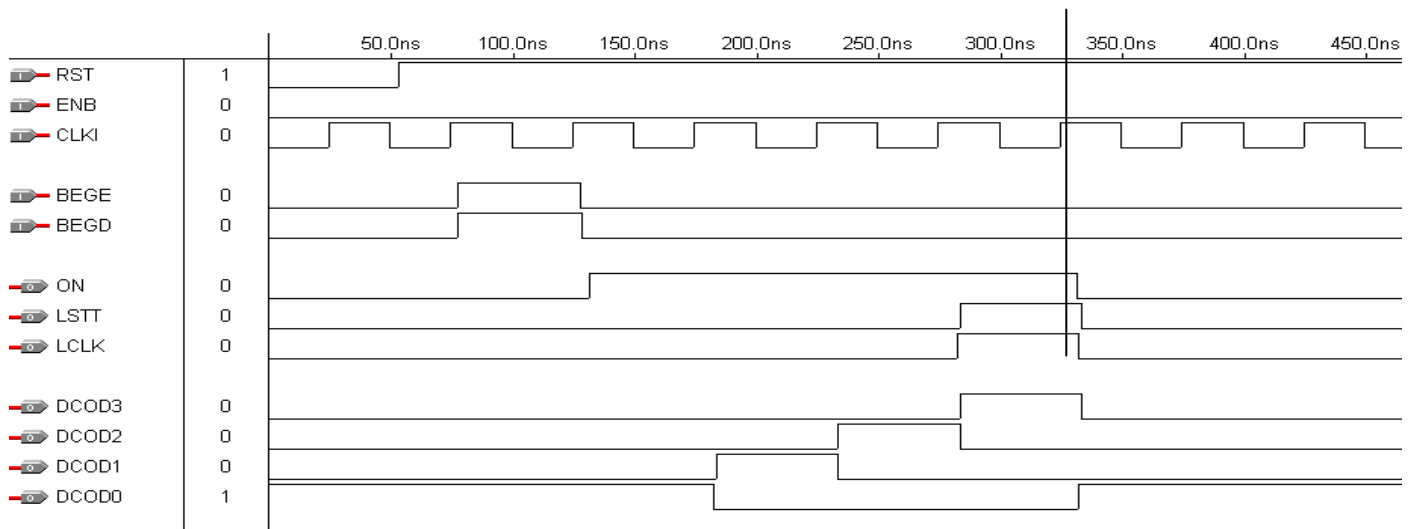
ENTITY MYTOP IS
    PORT (
        BEG      :IN      NODE;
        CLKI     :IN      NODE:= '1';
        RST      :IN      NODE:= '1';
        PRN      :IN      NODE:= '1';
        LSTT     :BUFFER  NODE;
        LCLK     :BUFFER  NODE;
        DCOD     :BUFFER  BUS1D(WDO-1 DOWNT0 0);
        SCNT     :BUFFER  BUS1D(WDL-1 DOWNT0 0);
        SON      :BUFFER  NODE;
    );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS
BEGIN

A1: S_TATE GENERIC MAP(CNT=>4,WD0=>16,WDL=>4)
    PORT      MAP(BEG,BEG,CLKI,RST,'1','0',LSTT,LCLK,DCOD,ON);
END MYTOP;

```

## TIMING DIAGRAM – Sample Design-1



## SAMPLE DESIGN-2

```

LIBRARY IEEE;

```

```

USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
    PORT (
        CLKI :IN      NODE:= '1';
        RST  :IN      NODE:= '1';
        ENB  :IN      NODE:= '1';
        LSTT :BUFFER NODE;
        LCLK :BUFFER NODE;
        DCOD :BUFFER BUS1D(WDO-1 DOWNT0 0);
        ON   :BUFFER NODE;
    );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS
BEGIN

A1: S_TATE GENERIC MAP(CNT=>4,WD0=>16)
    PORT MAP('0','0',CLKI,RST,ENB,LSTT,LCLK,DCOD,ON);
END MYTOP;

```

### **TIMING DIAGRAM – Sample Design-2**

