VLSI DESIGN OF SERIAL FLASH INTERFACE CONTROLLER

An important feature in most electronic systems is the ability to store data to non-volatile memory. As systems get smaller, cheaper, mobile and battery powered, the requirement of devices with smaller Form Factors, lower power consumption and faster access, increases. Serial Flash memories, fit this requirement perfectly.

The S_PIF.VHD IP core, described here, is an interface controller for 8 bit Serial Flash memories with an SPI bus interface. It can be implemented as a descrete device in an FPGA/CPLD or ASIC.

This core provides all the necessary interface logic for SPI Flash memories with an interface protocol compatible with MP45PE10 from SGS Thompson., freeing embedded software of interfacing tasks. TRI-STATE outputs permit implementation as a discrete device on an external data bus. Flexible bus width permits interface with a variety of processors. Synchronous design using a single global clock, ensures reliable operation over a range of clock frequencies and temperature.

FEATURES

- **Double buffered interface logic** allows configuration to **any bus width,** from **serial** to **parallel** of any width.
- Interface on data bus or port, **dedicated or shared.**
- Implements **SPI bus** protocol without program intervention
- Configurable **Serial Clock** frequency.
- **TRI-STATE** outputs for implementation as a **descrete device ASIC** or **PLD.**
- **Any clock frequency**

APPLICATION

Used as a solid state hard disk in a variety of applications
consumer electronic products such as :-

- Flash disks
- Memory sticks
- iPODs
- Refigerators
- Microwave ovens
- Mobile Phones
- Automotive electronics

Industrial and commercial control applications such as:-

- Motor (AC/DC)
- Power (AC/DC)
- Robotics
- Data-Loggers
- Osciloscopes, Spectrum and logic analysers
- Electronic Meters

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VHDL Component Declaration:

```
COMPONENT S_PIF
      GENERIC (
            S_FLM  :INTEGER := 1;
            EBUS   :INTEGER := 1;
            DBW    :INTEGER := 8;
            MXW    :INTEGER := 5;
            MXR    :INTEGER := 2;
            GCL    :INTEGER := 20000000;
            SCKF   :INTEGER := 5000000
      );
      PORT(
            CLKI   :IN     NODE;
            RST    :IN     NODE;
            RD     :IN     NODE;
            WR     :IN     NODE;
            A0     :IN     NODE;
            SERI   :IN     NODE;
            DIN    :IN     BUS1D(NTI(DBW) DOWNTO 0);
            DOUT   :BUFFER BUS1D(NTI(DBW) DOWNTO 0);
            SCLO   :BUFFER NODE;
            SERO   :BUFFER NODE;
            CS     :BUFFER NODE
      );
END COMPONENT;
```

FILES YOU GET

```
   i)FUNC.DOC        -     Documentation of functions & data types used in the core.
  ii)README.DOC      -     Compile and licensing information.
 iii)ADC.DOC         -     This document

 a)MYLIB.VHD         -     PACKAGE
 b)S_PIF.VHD         -     TOP HIERARCHY DESIGN FILE
 c)T_RI.VHD          -     DESIGN FILE BELOW TOP HIERARCHY
 d)M_TRI.VHD         -           -DO-
 e)D_BIR.VHD         -           -DO-
 f)M_DFF.VHD         -           -DO-
 g)S_DFF.VHD         -           -DO-
 h)F_IFO.VHD         -           -DO-
 i)D_ECOD.VHD        -           -DO-
 j)P_AD.VHD          -           -DO-
 k)P_DV.VHD          -           -DO-
 l)P_LSE.VHD         -           -DO-
 m)D_BIL.VHD         -           -DO-
 n)F_DIV.VHD         -           -DO-
 o)U_DCNT.VHD        -           -DO-
 p)I_NCDEC.VHD       -           -DO-
 q)A_DSB.VHD         -           -DO-
 r)S_TFF.VHD         -           -DO-
 s)S_JKF.VHD         -           -DO-
 t)B_SHIFT.VHD       -           -DO-
 u)R_STK.VHD         -           -DO-
```


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INTERFACE INFORMATION

The schemes described here provide information on interfacing this core with other peripherals on a common data bus & ports.

The data bus and port can be of any size and can be shared with any number of peripherals. The Read (RD) and Write (WR) lines must be unique for this core. These signals can be generated either by an i/o address decoder, within the PLD (in the bus interface schemes) or from an output port on a micro-controller (in the port interface schemes).

Read data is sent by the core to the CPU while the RD input is Hi and Write data is loaded into the core while the WR input is Hi. Read data can be taken outside the PLD, to an external data bus or port, if the EBUS parameter is set to one. When EBUS=1, data is routed through TRI-STATE buffers. the Output Enable of each of these buffers is the RD input. When EBUS=0, data is routed to the internal read port after ANDing with the RD signal ie TRI-STATE buffers are not used.

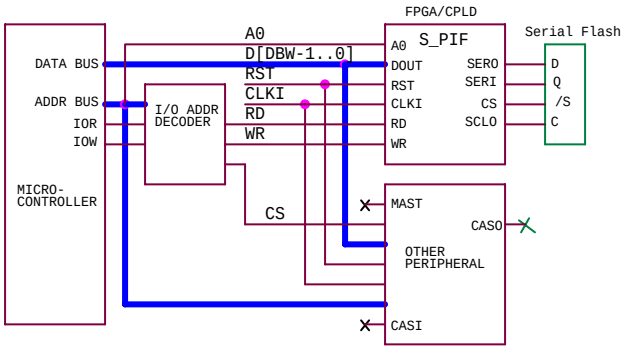
The CPU communicates with the Flash memory device by writing and reading data to and from the internal registers of the S_PIF core. The register selected, its size and the action performed depends on the combination of the RD,WR and A0 inputs (see tables 4,5 and 6).

If the size of the data bus or port is less than the size (RWD) of these registers, data from and to the CPU is sliced to NSD slices. The CPU must then send the MSB slice first and continue to send subsequent slices till the entire contents of the register are transferred. When reading, the CPU will receive the MSB slice first and then the subsequent slices, contiguously, until the entire contents of the register are transferred. Since the maximum value of RWD=8, if the data bus/port width is 8 bits or more, slicing is not performed. The calculation of NSD is shown in the section on "S_PIF Register Structure"

CIRCUIT DIAGRAMS

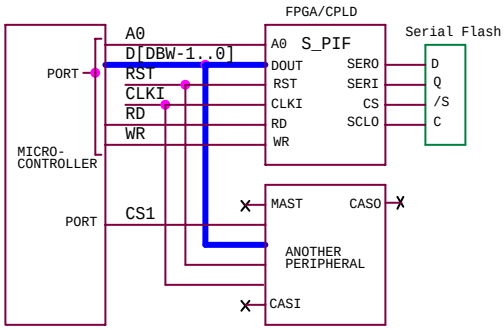
EXTERNAL DATA BUS

Parameter EBUS=1

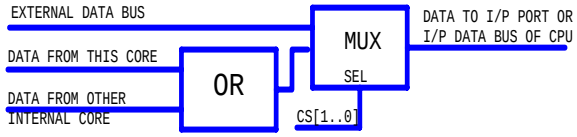


EXTERNAL PORT

Parameter EBUS=1



CONNECTION OF INTERNAL CORES TO CPU



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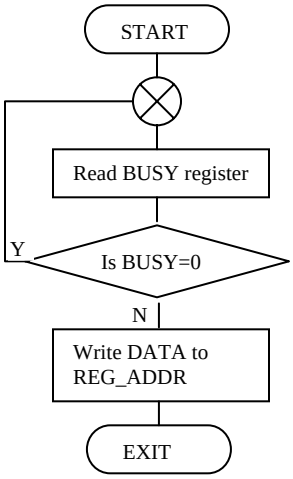
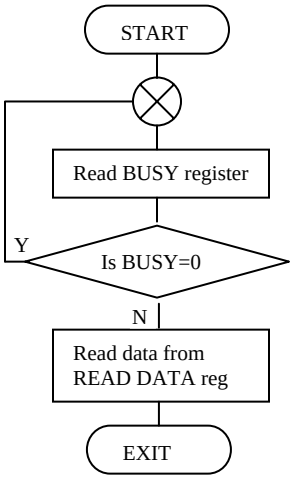
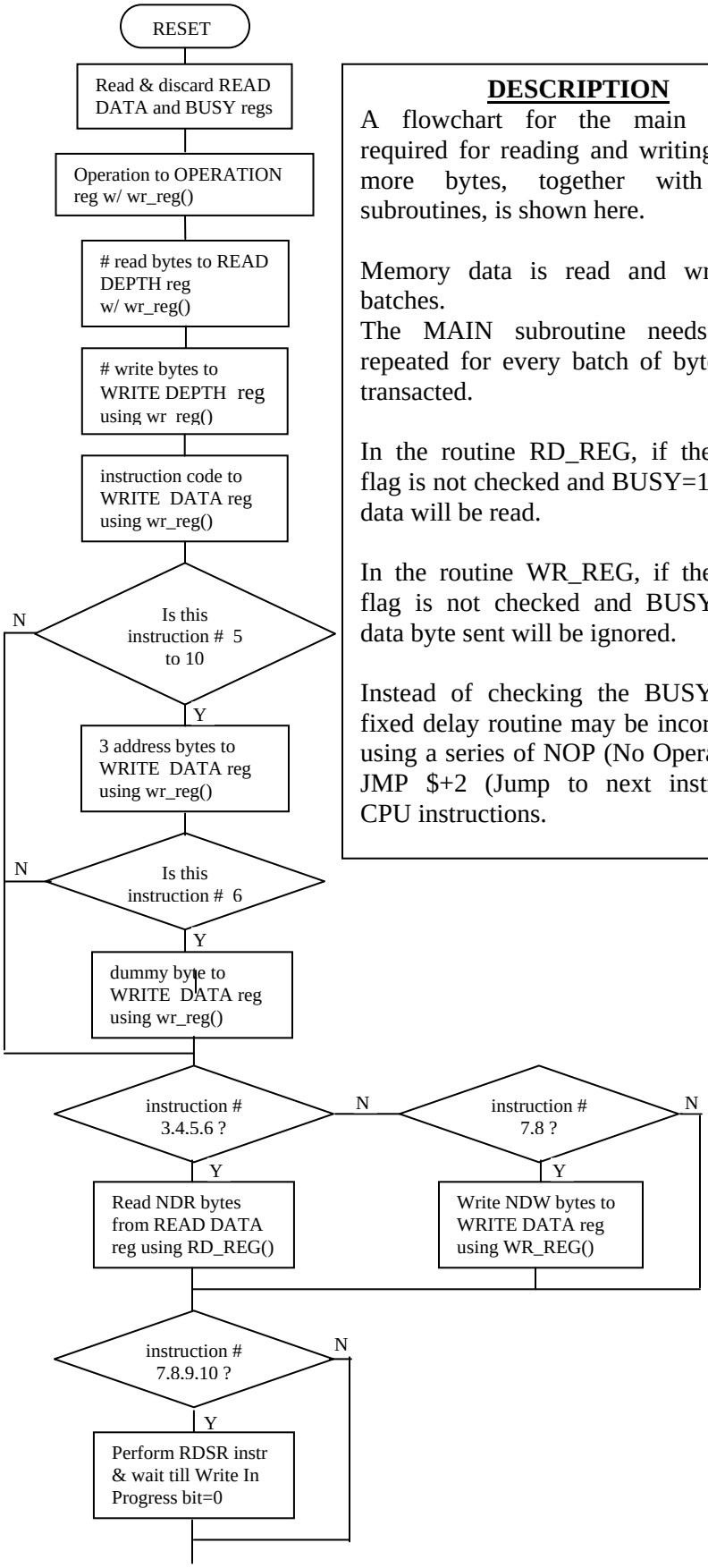
FLOW CHART FOR FUCTION WR_REG(DATA,REG_ADDR)



FLOW CHART FOR FUCTION RD_REG()



FLOW CHART FOR MAIN PROGRAM



DESCRIPTION

A flowchart for the main function required for reading and writing one or more bytes, together with called subroutines, is shown here.

Memory data is read and written in batches.
The MAIN subroutine needs to be repeated for every batch of bytes to be transacted.

In the routine RD_REG, if the BUSY flag is not checked and BUSY=1, invalid data will be read.

In the routine WR_REG, if the BUSY flag is not checked and BUSY=1, the data byte sent will be ignored.

Instead of checking the BUSY flag a fixed delay routine may be incorporated, using a series of NOP (No Operation) or JMP $+2 (Jump to next instruction), CPU instructions.

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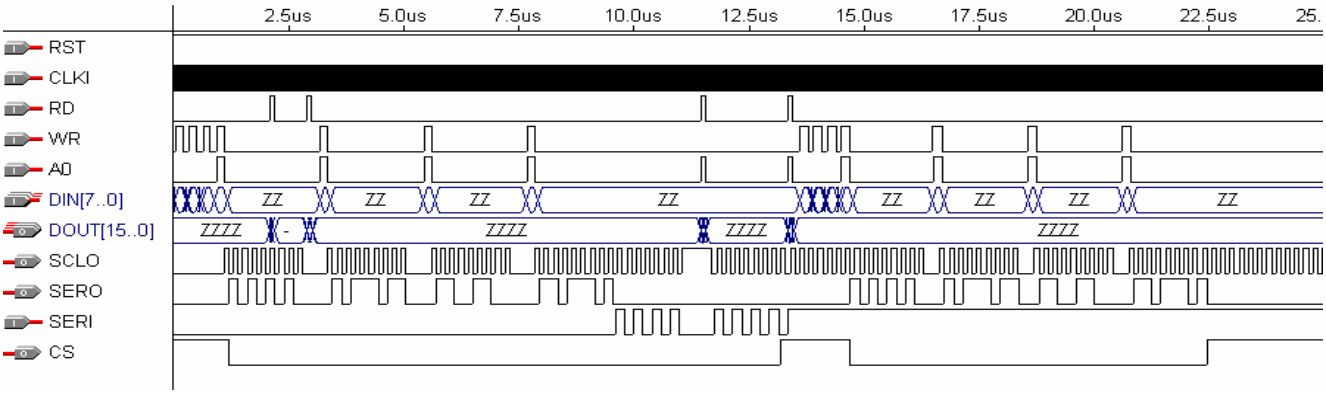
END

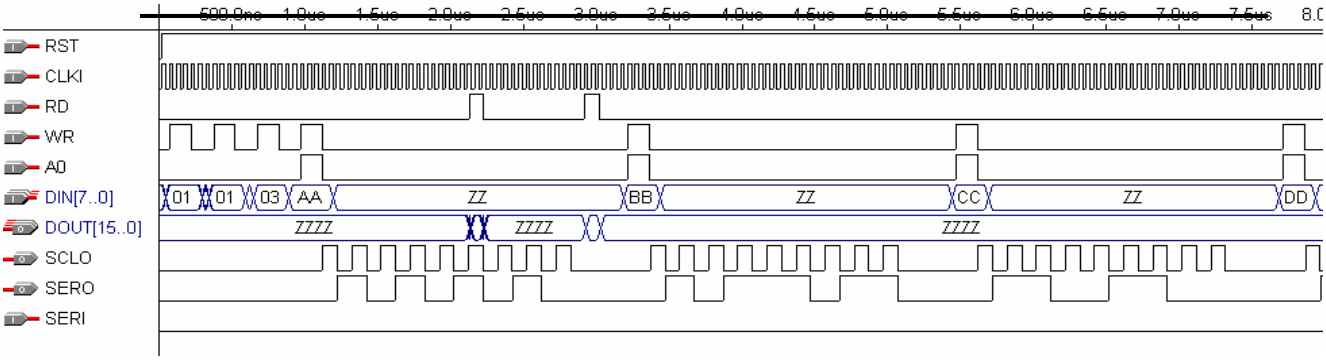
SAMPLE DESIGN-1

```
LIBRARY  IEEE;
USE  IEEE.STD_LOGIC_1164.ALL;
USE  IEEE.STD_LOGIC_ARITH.ALL;
USE  IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY  MYLIB;
USE  MYLIB.MYLIB.ALL;

ENTITY  MYTOP  IS
     PORT(
          CLKI     :IN     NODE;
          RST      :IN     NODE;
          RD       :IN     NODE;
          WR       :IN     NODE;
          A0       :IN     NODE;
          SERI     :IN     NODE;
          DIN      :IN     BUS1D(15 DOWNTO 0);
          DOUT     :BUFFER BUS1D(15 DOWNTO 0);
          SCLO     :BUFFER BUS1D(0 DOWNTO 0);
          SERO     :BUFFER NODE;
          CS       :BUFFER NODE;
     );
END  MYTOP;

ARCHITECTURE   MYTOP  OF  MYTOP  IS
BEGIN
A1: S_PIF GENERIC MAP (
                        EBUS=>1,              --DOUT connected to external data bus
                        DBW =>8,              --16 bit data bus width
                        MXW =>5,              --16 bit data bus width
                        MXR =>2,              --16 bit data bus width
                        GCL =>20000000,       --20 MHz clock i/p
                        SCKF=>5000000)        --T_tr delay of Converter

          PORT MAP    (CLKI,RST,RD,WR,A0,SERI,DIN,DOUT,SCLO,SERO,CS);
END  MYTOP;
```

SAMPLE DESIGN-1 TIMING DIAGRAMS



DETAILED VIEW 0 TO 8us



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DETAILED VIEW 8us TO END

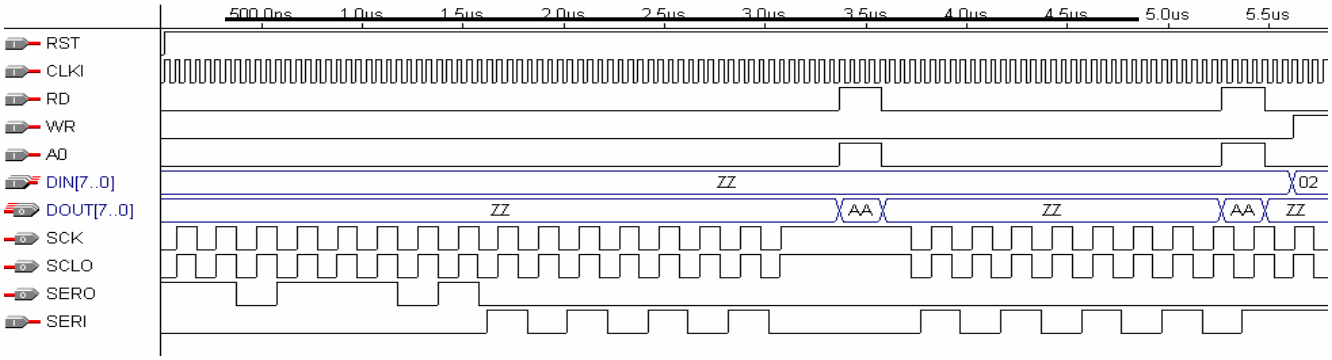

Table 0 **FLASH MEMORY INSTRUCTION SET**

SR	NEMONIC	DESCRIPTION	Inst Code (HEX)	Address Write Bytes-NAD	Dummy Write Bytes-NDM	Data Read Bytes-NDR	Data Write Bytes-NDW
1	WREN	Write enable	06	0	0	0	0
2	WRDI	Write disable	04	0	0	0	0
3	RDID	Read ID	9F	0	0	1 to 3	0
4	RDSR	Read Status Reg	05	0	0	1 to ∞	0
5	READ	Read Data Bytes	03	3	0	1 to ∞	0
6	FAST_READ	Fast Read	0B	3	1	1 to ∞	0
7	PW	Page Write	0A	3	0	0	1 to 256
8	PP	Page Program	02	3	0	0	1 to 256
9	PE	Page Erase	DB	3	0	0	0
10	SE	Sector Erase	D8	3	0	0	0
11	DP	Deep Power Dn	B9	0	0	0	0
12	RDP	Release Deep Power Dn	AB	0	0	0	0

S_PIF - INTERNAL REGISTERS

Table 4-**READ REGISTERS**

NAME	WIDTH (RWD)	WR	RD	A0	READ ORDER	DESCRIPTION
BUSY	1	0	1	0	Random	When 0, READ DATA register contains valid data else invalid.
READ DATA	8	0	1	1	Random	Memory data
-	-	0	0	X	-	Invalid combination

Table 5-**WRITE REGISTERS**

NAME	WIDTH (RWD)	RD	WR	A0	WRITE ORDER	DESCRIPTION
OPERATION	2	0	1	0	1st	Specifies type of current instruction (see table 6)
READ DEPTH	1+Log2 (MXR-1)	0	1	0	2nd	# bytes read (NDR-1) from Flash, in current instruction. See Table 0
WRITE DEPTH	1+Log2 (MXW-1)	0	1	0	3rd	# bytes written (NAD+NDM+NDW) to Flash in current instruction (Table 0)
WRITE DATA	8	0	1	1	4th onward	Instruction bytes followed by memory write data, if any. Instruction bytes-One Instruction code byte followed by NAD Address bytes and NDM Dummy bytes. Ref table 0
-	-	0	0	X	-	Invalid combination

Table 6-**OPERATION REGISTER**

BIT 1	BIT 0	DESCRIPTION
0	0	Invalid
0	1	current operation is a read from memory
1	0	current operation is a write from memory
1	1	Invalid

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PARAMETERS AND PORTS

Table 2-**OUTPUT_PORTS**

NAME	DESCRIPTION	WIDTH	COMMENTS
DOUT	Data bus	DBW	Bus containing data Read by a CPU from the internal registers of S_PIF. When EBUS=1, it is bi-directional, fed by TRI-STATE buffers, enabled with the 'RD' input, also used for input data instead of the DIN input port. When EBUS=0, it is uni-directional and data is output on it without TRI buffers and DIN is used as an input. The register selected for output data, depends on the A0 port (see table 4).
CS	Chip Select	1	Active Lo, Flash Memory Chip Select, connected to the '/S' pin of the Flash device
SCLO	Serial Clock	1	Serial clock. Connect to 'C' pin of Flash device
SERO	Serial data out	1	Serial data output. Connect to 'D' pin of Flash device.

Table 1-**INPUT_PORTS**

NAME	DESCRIPTION	WIDTH	COMMENTS
DIN	Input data bus	DBW	Parallel data bus containing data sent by the CPU to S_PIF. Used only when EBUS=0. When EBUS=1, input data is taken from the DOUT port.
A0	Register select	1	In combination with RD, WR selects an internal register for Read or Write operation. Must be coincident with RD and WR. See table 5
CLKI	Clock	1	Positive edge triggered. Synchronizes all internal operations.
RST	Reset	1	Active lo, asynchronous, resets all internal logic
SERI	Serial data in	1	Serial data in. Connect to 'Q' pin of Flash device.
RD	Read	1	Active Hi, Read command from CPU. In combination with the A0 port, selects an internal register and sends its data to the DOUT output port. Hi time >=1 CLKI Lo time >=3 CLKI (NSD>1) Lo time >=1 CLKI (NSD=1)
WR	Write	1	Active Hi, Write command from CPU. In combination with the A0 port, selects an internal register and loads it with the contents of the DIN input port. Hi time is atleast one CLKI period. See table 5

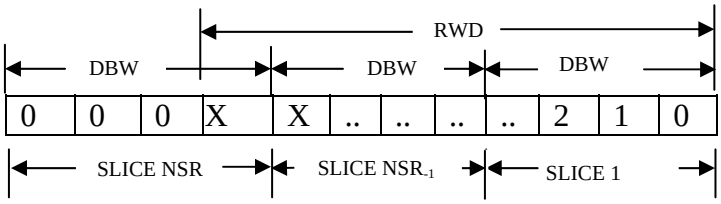
Table 3-**PARAMETERS**-all INTEGER type(Minimum value-0)

NAME	MIN	DESCRIPTION
EBUS	0	When EBUS=1, DOUT is a bi-directional used for o/p and i/p (instead of the DIN port). When EBUS=0, DIN and DOUT are dedicated uni-directional ports.
S_FLM	1	Reserved. Leave 1 or unused
DBW	1	Width of DIN input port and DOUT output port
GCL	2	Frequency of CLKI input
SCKF	1	Frequency of SCLO output when SCKF<=GCL/2. See Flash device specs
MXW	NAD+NDM+NDW+1	Maximum number of instruction and data bytes, written to Flash device. See Table 0
MXR	NDR	Maximum number of data bytes, read from Flash device. See Table 0

S_PIF - INTERNAL REGISTER STRUCTURE (ref Table 4 & 5)

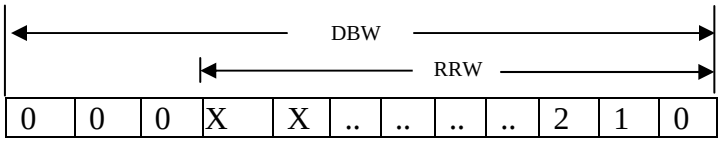
When DBW>RWD, data is not sliced, otherwise data is sent or recieved in NSD slices.

DBW< RWD



NSD=INT(RWD/DBW) (if remainder>0, add 1)

DBW>= RWD



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