



## S\_LCH

**DESCRIPTION** –D latch with clear, preset and enable.

### **VHDL Component Declaration:**

```
COMPONENT S_LCH
  PORT (D      :IN  NODE:= '0';
        ENB    :IN  NODE:= '1';
        CLR    :IN  NODE:= '1';
        PRN    :IN  NODE:= '1';
        Q      :BUFFER NODE;
  );
END COMPONENT;
```

### **FILES YOU GET**

- i) FUNC.DOC – Documentation of functions & data types used in the core.
- ii) README.DOC – Compile and licensing information.
- iii) SLCH.DOC – This document
  
- a) MYLIB.VHD – PACKAGE
- b) S\_LCH.VHD – TOP HIERARCHY DESIGN FILE

### **INPUT PORTS**

Name	Required	Description	Comments
D	No	Data input	
ENB	Yes	Latch enable input.	High=flow-through, Low=latch.
CLR	No	Asynchronous clear	Active lo, default=1. Sets the latch to all 0's. If PRN and CLR are used and both are asserted, CLR is dominant
PRN	No	Asynchronous preset	Active lo, default=1. Sets latches to all 1's. If PRN and CLR are used and both are asserted, CLR is dominant

### **OUTPUT PORTS**

Name	Required	Description	Comments
Q	Yes	Latched output	W+1 bits wide.

### **FUNCTION**

CLR	PRN	ENB	Q[W..0]
L	X	X	000...
H	L	X	111...
L	L	X	000...
H	H	L	Q[] (no change)
H	H	H	D[]=>Q[]

### **SAMPLE DESIGN**



```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
  PORT(ENB      :IN  NODE;
        CLR     :IN  NODE;
        PRN     :IN  NODE;
        D       :IN  NODE;
        Q       :BUFFER NODE
  );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

BEGIN

A1: S_LCH PORT MAP (D,ENB,CLR,PRN,Q);

END MYTOP;
```