



S_JKF

DESCRIPTION –JK flip-flop with clear, preset and enable.

VHDL Component Declaration:

```
COMPONENT S_JKF
  PORT (J      :IN  NODE:= '0';
        K      :IN  NODE:= '0';
        CLKI   :IN  NODE:= '1';
        CLR    :IN  NODE:= '1';
        PRN    :IN  NODE:= '1';
        ENB    :IN  NODE:= '1';
        Q      :BUFFER NODE;
  );
END COMPONENT;
```

FILES YOU GET

- i) FUNC.DOC - Documentation of functions & data types used in the core.
- ii) README.DOC - Compile and licensing information.
- iii) SJKF.DOC - This document

- a) MYLIB.VHD - PACKAGE
- b) S_JKF.VHD - TOP HIERARCHY DESIGN FILE
- c) S_DFF.VHD - DESIGN FILE BELOW TOP HIERARCHY

INPUT PORTS

Port Name	Required	Description
J	Yes	J input to flipflop
K	Yes	K input to flipflop
CLKI	Yes	Positive edge triggered clock.
CLR	No	Clear, active low,clears flipflops to low.
PRN	No	Preset, active low, presets flipflops to hi
ENB	No	Clock enable, output remains frozen when low.

OUTPUT PORTS

Port Name	Required	Description
Q	Yes	Data output from flipflops



FUNCTION

J	K	CLR	CLKI	PRN	ENB	Q
X	X	L	X	X	X	L
X	X	H	X	L	X	H
X	X	L	X	L	X	illegal
X	X	H	X	H	L	Q (no change)
H	L	H	↑	H	H	H
L	H	H	↑	H	H	L
H	H	H	↑	H	H	Toggle
L	L	H	X	H	H	Q (no change)

SAMPLE DESIGN

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
    PORT(CLKI    :IN  NODE;
          CLR     :IN  NODE;
          PRN     :IN  NODE;
          J       :IN  NODE;
          K       :IN  NODE;
          Q       :BUFFER NODE
    );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

BEGIN

A1: S_JKF PORT MAP (J,K,CLKI,CLR,PRN,ENB,Q);

END MYTOP;
```