



S_DFF

DESCRIPTION –D flip-flop with clear, preset and enable.

VHDL Component Declaration:

```
COMPONENT S_DFF
  PORT (D      :IN  NODE:= '0';
        CLKI   :IN  NODE:= '1';
        CLR    :IN  NODE:= '1';
        PRN    :IN  NODE:= '1';
        ENB    :IN  NODE:= '1';
        Q      :BUFFER NODE;
  );
END COMPONENT;
```

FILES YOU GET

- i) FUNC.DOC - Documentation of functions & data types used in the core.
- ii) README.DOC - Compile and licensing information.
- iii) S_DFF.DOC - This document

- a) MYLIB.VHD - PACKAGE
- b) S_DFF.VHD - TOP HIERARCHY DESIGN FILE

INPUT PORTS

Port Name	Required	Description
D	Yes	Data input to flipflop
CLKI	Yes	Positive edge triggered clock, Q output changes to D at rising edge
CLR	No	Asynchronous clear, active low,clears flipflop to low.
PRN	No	Asynchronous preset, active low, presets flipflop to hi
ENB	No	Clock enable, output remains frozen when low.

OUTPUT PORTS

Port Name	Required	Description
Q	Yes	Data output from flipflop



FUNCTION

CLR	CLKI	PRN	ENB	Q
L	X	X	X	L
H	X	L	X	H
L	X	L	X	illegal
H	X	H	L	Q (no change)
H	↑	H	H	D=>Q

SAMPLE DESIGN

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
  PORT(CLKI :IN NODE;
        CLR  :IN NODE;
        PRN  :IN NODE;
        D    :IN NODE;
        Q    :BUFFER NODE
  );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

BEGIN

A1: S_DFF PORT MAP (D,CLKI,CLR,PRN,ENB,Q);

END MYTOP;
```