



# R\_TCC

## DESCRIPTION – Real Time Clock and Calender

The R\_TCC.VHD IP core, described here, is a real time clock and calender. This core combines a complete time-of-day clock with an over hundred year (configurable) calender. It may be used with any microprocessor to relieve the software of timekeeping workload. TRI-STATE outputs are provided for easy bus operation.

## FEATURES

- Automatic **End of Month Recognition**
- Automatic **Leap Year Compensation**
- Counts **Seconds, Minutes** and **Hours** of day
- Counts Days of Week, **Date, Month** and **Year**.
- Once per second **Interrupt** output.
- **Double buffered interface logic** allows configuration to any bus width, from **serial** to **parallel** of any width.
- Interface on data bus or port, **dedicated or shared**.
- Instantiate the core as **stand-alone** or **cascaded**, in a daisy chain configuration.
- **Daisy chain** multiple **cores** on **one port address**.
- Configure for any number of **Years**.
- Can be configured for **any clock frequency**

## APPLICATION

Date and Time information for a host of portable and battery powered, commercial and industrial goods:-

- Data loggers such as:-
  - Gas Analyser
  - pH Analyzer
  - Attendance recorders
  - Power Meters
- Cheque readers
- Magnetic card readers
- Medical equipment-ECG,EKG
- Computers
- Mobile Phones



## **VHDL Component Declaration:**

```
COMPONENT R_TCC
  GENERIC (
    EBUS   : INTEGER:=1;
    DBW    : INTEGER:=16;
    LYR    : INTEGER:=63;
    CSCR   : INTEGER:=1;
    CSCW   : INTEGER:=1;
    RTC    : INTEGER:=1;
    CEF    : INTEGER:=0;
    GCL    : INTEGER:=20000000
  );
  PORT (
    MSTR   : IN           NODE:='1';
    MSTW   : IN           NODE:='1';
    CSIR   : IN           NODE:='0';
    CSIW   : IN           NODE:='0';
    CLKI   : IN           NODE:='0';
    RST    : IN           NODE:='1';
    A0     : IN           NODE:='0';
    WR     : IN           NODE:='0';
    RD     : IN           NODE:='0';
    DIN    : IN           BUS1D(DBW-1 DOWNT0 0):=(OTHERS=>'0');
    CLKEN  : IN           NODE:='1';
    CNTEN  : IN           NODE:='1';
    DOUT   : INOUT       BUS1D(DBW-1 DOWNT0 0);
    CSOR   : BUFFER      NODE;
    CSOW   : BUFFER      NODE
  );
END COMPONENT;
```

## **FILES YOU GET**

i) FUNC.DOC	-	Documentation of functions & data types used in the core.
ii) README.DOC	-	Compile and licensing information.
iii) RTCC.DOC	-	This document
a) MYLIB.VHD	-	PACKAGE
b) R_TCC.VHD	-	TOP HIERARCHY DESIGN FILE
c) M_DFF.VHD	-	DESIGN FILE BELOW TOP HIERARCHY
d) S_DFF.VHD	-	-DO-
e) P_AD.VHD	-	-DO-
g) I_NCDEC.VHD	-	-DO-
h) U_DCNT.VHD	-	-DO-
i) A_DSB.VHD	-	-DO-
j) D_BIL.VHD	-	-DO-
k) S_TFF.VHD	-	-DO-
l) S_JKF.VHD	-	-DO-
m) F_DIV.VHD	-	-DO-
n) B_SHIFT.VHD	-	-DO-
o) D_EC0D.VHD	-	-DO-
p) P_LSE.VHD	-	-DO-
r) M_TRI.VHD	-	-DO-
s) S_TRI.VHD	-	-DO-
t) F_IFO.VHD	-	-DO-
u) D_BIR.VHD	-	-DO-
v) C_SIO.VHD	-	-DO-
w) R_STK.VHD	-	-DO-



## **INTERFACE INFORMATION**

The interface schemes described here provide the user with information on how this core can be interfaced along with other peripherals on the common system resources, such as the data bus and input ports.

The two types of interface schemes are described here are:-

- 1) **Cascaded** - (read or write)
- 2) **Stand-alone** - (read or write)

In all the interface schemes the data bus and port can be shared with any number of peripherals. However the Chip Select line (CS) must be unique for every core instantiated in the stand-alone scheme and common to all cascaded cores instantiated in the cascaded interface scheme. Chip-select signals can be generated either by an i/o address decoder, within the PLD(in the bus interface schemes) or from an output port on a micro-controller(in the port interface schemes).

Read and Write operations can be connected in any combination of Cascade and stand-alone, Read may be cascaded and Write stand-alone or Write cascaded and Read stand-alone or both cascaded or both stand-alone.

### **READ**

The number of bits of data transmitted, at a time, by the core to the CPU, depends on the number of data lines connected to the core. If the number of data lines connected is less than that required for a full parallel transmission, data is sliced to the size of the data lines. The sliced data must be read contiguously until the whole data word is assembled by the CPU. Calculation of the number of slices of data (NSR) is shown below.

The DOUT port can be taken outside the PLD if the EBUS parameter is set to one, data is then routed through TRI-STATE buffers, which are enabled when the core is enabled with its RD input. The OEN (output enable) signal of these buffers is coincident with the RD input.

Data reading order is as follows:- SEC first then MIN, HRS, DAY, MTH and YRS. MSB slice of each field is read first.

### **WRITE**

The number of bits of data transmitted, at a time, by the CPU to the core, depends on the number of data lines connected to the core. If the number of data lines connected is less than that required for a full parallel transmission, data is sliced to the size of the data lines. The sliced data must be sent contiguously until the whole data word is assembled by the core. Calculation of the number of slices of data (NSW) is shown below.

Data writing order is as follows:- When writing date, send DAY then MTH and last YRS. When writing time, send SEC then MIN and last HRS MSB slice of each field should be written first.



## **CASCADED**

In cascaded interface, although the chip select logic overhead is minimum, the cores cannot be accessed randomly and must be accessed sequentially one after the other and the entire sequence must be completed everytime, a process known as daisy chaining.

### **CASCADED READ**

The core, configured as the master will transmit first followed by the next in the chain. After a core transmits its data, it pulses the CSOR output, which being connected to the next core in the chain, enables it for data transmission. After all the cores in the chain are read, the master is once again enabled.

Cascading for read operations is enabled by setting the CSCR parameter to one and connecting the MSTR input of the first core in the chain to '1' and the CSOR output of each core to the CSIR input of the next core in the chain. The CSOR output of the last core in the chain is connected to the CSIR input of the master, or the first core in the chain.

### **CASCADED WRITE**

The core, configured as the master will load first followed by the next in the chain. After a core loads its data, it pulses the CSOW output, which being connected to the next core in the chain, enables it for data reception. After all the cores in the chain are loaded, the master is once again enabled.

Cascading for write operations is enabled by setting the CSCW parameter to one and connecting the MSTW input of the first core in the chain to '1' and the CSOW output of each core to the CSIW input of the next core in the chain. The CSOW output of the last core in the chain is connected to the CSIW input of the master, or the first core in the chain.

**In the cascaded write scheme either DATE or TIME, not both, can be written to in one scan of the cascade chain.**

## **STAND-ALONE**

In the stand-alone interface schemes, separate chip selects(RD/W) are required for each core. It gives the user, freedom of random access, however at the price of additional logic overhead and pinouts

### **STAND-ALONE READ**

The core is ready to transmit to the CPU soon after RST=1. The core with an active RD line will send data and only one core at a time must be activated. This option is enabled by setting the CSCR parameter to zero, the MSTR and CSIR inputs are not used and may be connected to any constant.

### **STAND-ALONE WRITE**

The core is ready to load data from the CPU soon after RST=1. The core with an active WR line will receive data and only one core at a time must be activated. This option is enabled by setting the CSCW parameter to zero, the MSTW and CSIW inputs are not used and may be connected to any constant.

### **WR TIMING REQUIREMENTS (CASCADED SCHEMES)**

- a) Frequency  $\leq 1/3$  of CLKI
- b) Hi time  $\geq 1$  CLKI
- c) Lo time  $\geq 1$  CLKI

### **RD TIMING REQUIREMENTS (CASCADED SCHEMES)**

- a) Hi time  $\geq 1$  CLKI
- b) Lo time  $\geq 2$  CLKI

### **RD/WR TIMING REQUIREMENTS (STAND-ALONE SCHEMES)**

- a) The RD/W signal of the next stand-alone core may come back to back after the RD/WR of the last slice of the previously selected core with no gap in between.
- b) Hi time of RD/WR  $\geq 1$  CLKI.



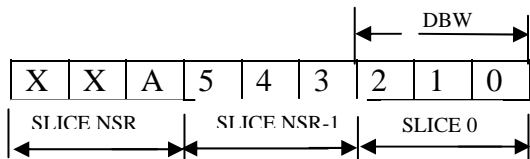
**CALCULATION OF NSR and structure of READ DATA**

**YEAR**

$A = \text{Log}_2(\text{LYR})$

$\text{NSR}_{\text{YR}} = [(A+1) / \text{DBW}] - 1$

If the result of division produces a remainder, add 1 to result  
 $\text{DBW} = 3$  for the examples shown below

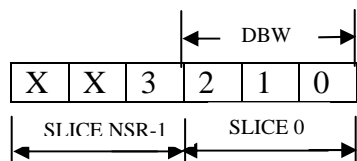


**EXAMPLE** - For LYR=100:-

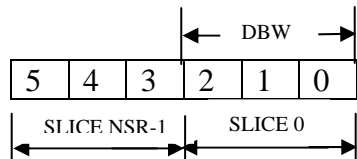
$A = \text{Log}_2(100) = 6$

$\text{NSR}_{\text{YR}} = [(6+1)/3]-1 = (2 \text{ rem } 1) - 1 = 2$

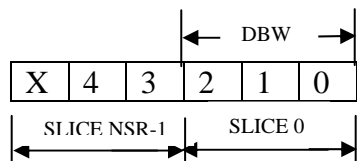
**MONTH** -  $\text{NSR}_{\text{MN}} = [4 / \text{DBW}] - 1 = 4/3 - 1 = (1 \text{ rem } 1) - 1 = 1$



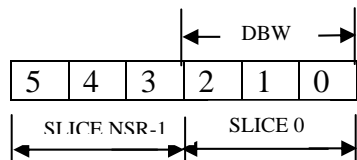
**DAY** -  $\text{NSR}_{\text{DY}} = [6 / \text{DBW}] - 1 = 6/3 - 1 = (2 \text{ rem } 0) - 1 = 1$



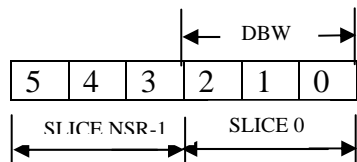
**HRS** -  $\text{NSR}_{\text{HR}} = [5 / \text{DBW}] - 1 = 5/3 - 1 = (1 \text{ rem } 1) - 1 = 1$



**MIN** -  $\text{NSR}_{\text{MN}} = [6 / \text{DBW}] - 1 = 6/3 - 1 = (2 \text{ rem } 0) - 1 = 1$



**SEC** -  $\text{NSR}_{\text{SC}} = [6 / \text{DBW}] - 1 = 6/3 - 1 = (2 \text{ rem } 0) - 1 = 1$





**CALCULATION OF NSW and structure of WRITE DATA**

**YEAR**

IF  $\text{Log}_2(\text{LYR}) < 5$

A=5

ELSE

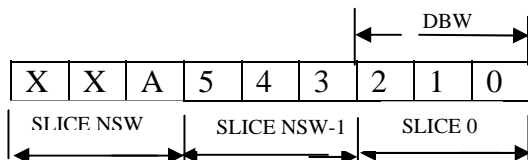
A=  $\text{Log}_2(\text{LYR})$

END IF

$\text{NSW}_{\text{YR}} = [(A+1) / \text{DBW}] - 1$

If the result of division produces a remainder, add 1 to result

DBW=3 for the examples shown below



**EXAMPLE** - For LYR=100:-

A =  $\text{Log}_2(100) = 6$

$\text{NSW}_{\text{YR}} = [(6+1)/3]-1 = (2 \text{ rem } 1) - 1 = 2$

**MONTH, DAY, HRS, MIN, SEC** -  $\text{NSW}_{\text{OTH}} = [6 / \text{DBW}] - 1 = 6/3 - 1 = (2 \text{ rem } 0) - 1 = 1$





## TIMING DIAGRAMS

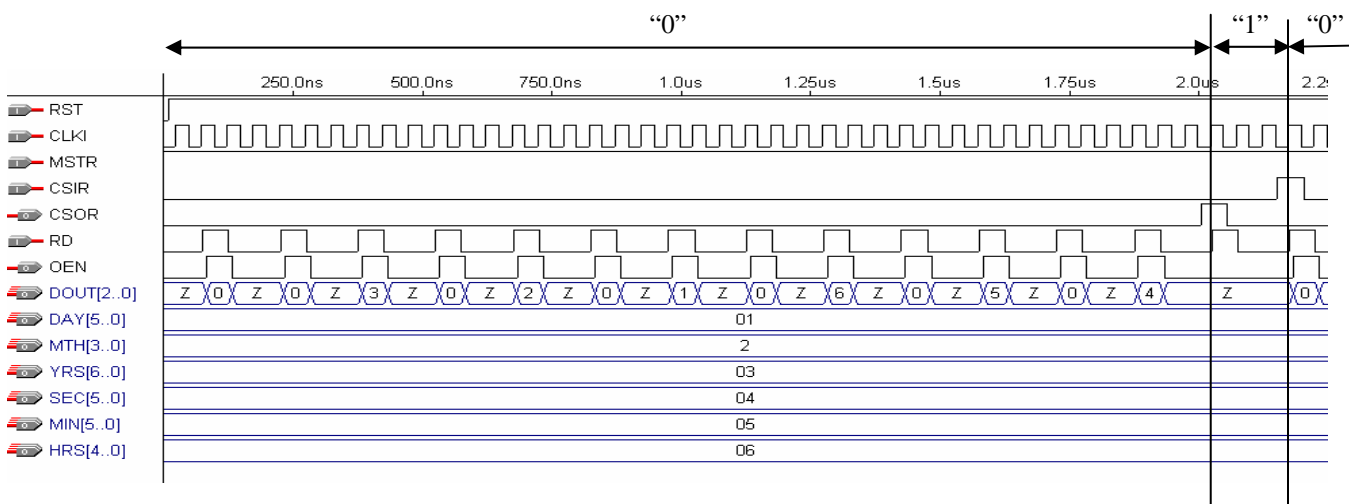
The EBUS parameter shown below may be 0 or 1. When EBUS=0 the OEN signal shown below is not present.

### CASCADED READ, CASCADED WRITE

Parameter Settings - EBUS=1/0,DBW=3,DBW=3,LYR=100,CSCR=1,CSCW=1,RTC=1,CEF=0,GCL=20000000

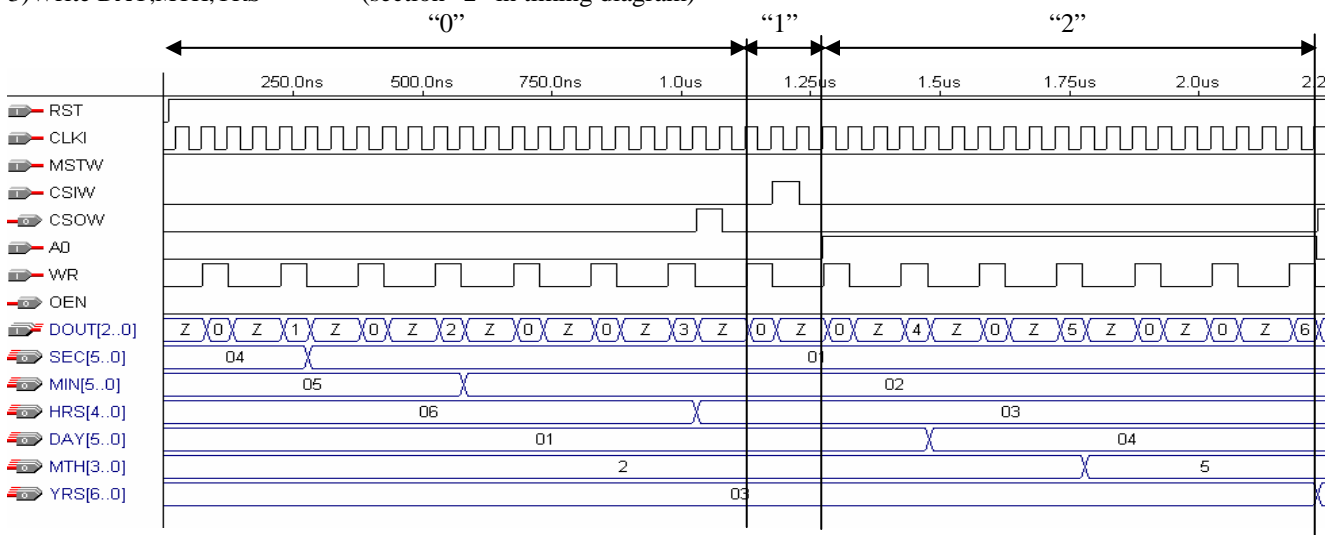
#### READ TIMING

- 1) Read YRS, MTH, DAY, HRS, MIN, SEC - (section "0" in timing diagram)
- 2) Read data from cascaded peripheral - (section "1" in timing diagram)



#### WRITE TIMING

- 1) Write SEC, MIN, HRS - (section "0" in timing diagram)
- 2) Write to cascaded peripheral - (section "1" in timing diagram)
- 3) Write DAY, MTH, YRS - (section "2" in timing diagram)



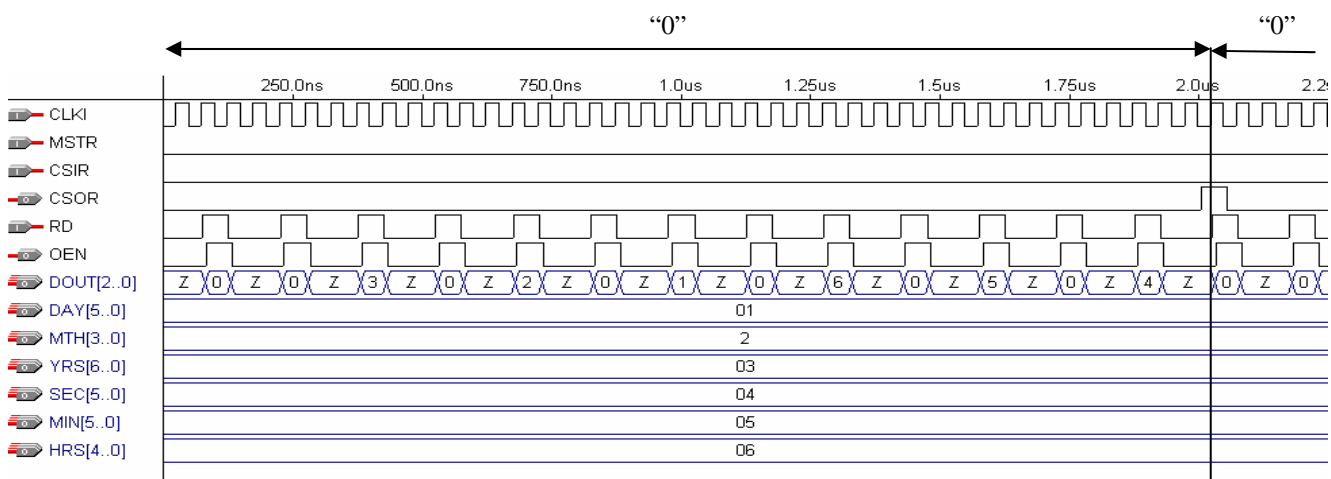


## 1b-STAND-ALONE READ, STAND-ALONE WRITE

Parameter Settings -EBUS=1/0,DBW=3,DBW=3,LYR=100,CSCR=0,CSCW=0,RTC=1,CEF=0,GCL=20000000

### READ TIMING

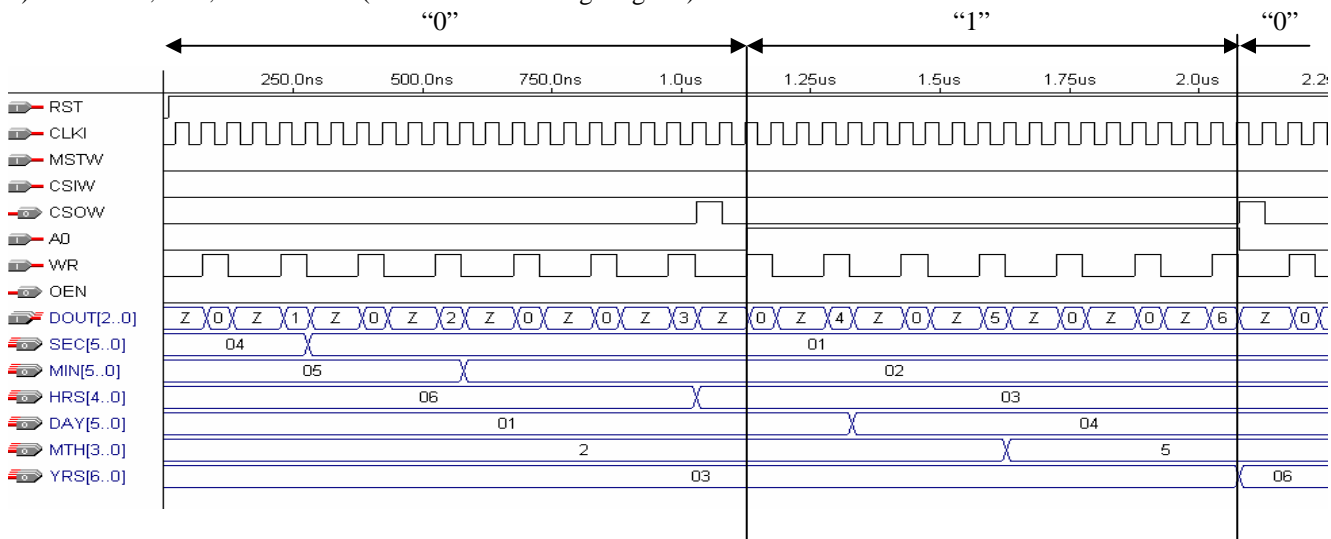
1)Read YRS,MTH,DAY,HRS,MIN,SEC - (section "0" in timing diagram)



### WRITE TIMING

1)Write SEC,MIN,HRS - (section "0" in timing diagram)

3)Write DAY,MTH,YRS - (section "1" in timing diagram)

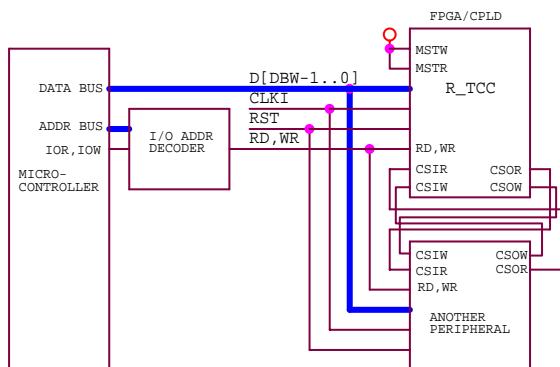




## CIRCUIT DIAGRAMS

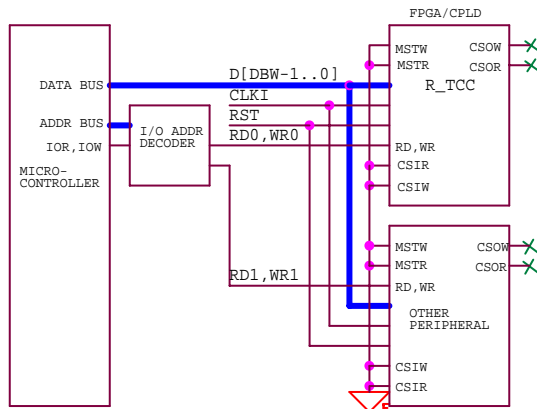
### EXTERNAL DATA BUS CASCADED READ, CASCADED WRITE

Parameters - CSCR=1,CSCW=1, EBUS=1



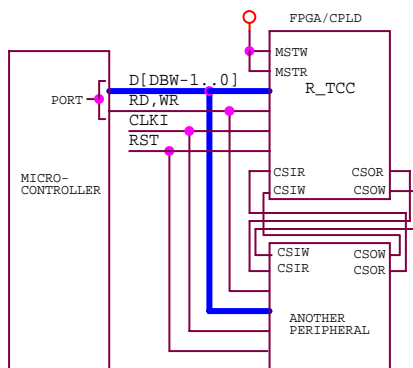
### EXTERNAL DATA BUS STAND-ALONE READ, STAND-ALONE WRITE

Parameters - CSCR=0,CSCW=0, EBUS=1



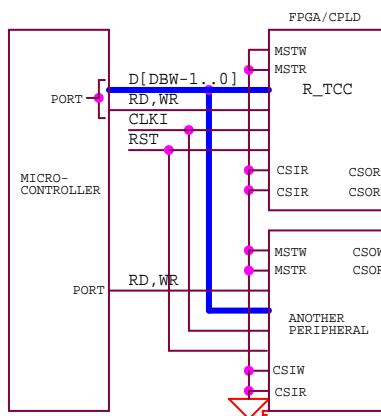
### EXTERNAL PORT CASCADED READ, CASCADED WRITE

Parameters - CSCR=1,CSCW=1, EBUS=1

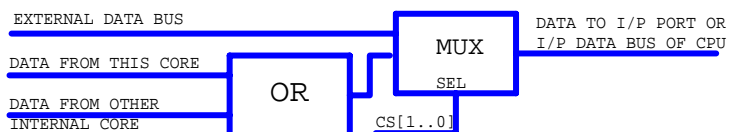


### EXTERNAL PORT STAND-ALONE READ, STAND-ALONE WRITE

Parameters - CSCR=0,CSCW=0, EBUS=1



### CONNECTION OF INTERNAL & EXTERNAL CORES TO CPU





## INPUT PORTS

NAME	DESC	WIDTH	COMMENTS
MSTR	Master select Read	1	When the core is a master, for read operations, in a cascaded configuration(CSCR=1), set MSTR to Hi. In a cascaded configuration if it is not the master, set it Lo. In a stand-alone configuration, it is unused and may be left open.
MSTW	Master select Write	1	When the core is a master for write operations, in a cascaded configuration (CSCW=1), set MSTW to Hi. In a cascaded configuration if it is not the master, set it Lo. In a stand-alone configuration, it is unused and may be left open.
CSIR	Cascade in Read	1	If the core is in a cascaded configuration(CSCR=1) and is not the master, for read operations, connect CSIR to the Cascade out port of the previous core in the chain, if it is the master, connect it to the cascade out of the last core in the chain. In a stand-alone configuration, for read operations, it is unused and may be left open.
CSIW	Cascade in Write	1	If the core is in a cascaded configuration(CSCW=1) and is not the master, for write operations, connect CSIW to the Cascade out port of the previous core in the chain, if it is the master, connect it to the cascade out of the last core in the chain. In a stand-alone configuration, for write operations, it is unused and may be left open.
A0	Address line	1	Write Time (A0=0) or Date (A0=1).
CLKI	Clock	1	Positive edge triggered. Synchronizes all internal operations
RST	Reset	1	Asynchronous, active lo, resets all internal logic
RD	Chip select Read	1	Active hi, enables the internal data read logic. Must be synchronous to the rising or falling edge of the CLKI input. The TRI-STATE buffers are enabled while RD is hi and RTCC data appears on the 'DOUT' port. <b>TIMING</b> (See 'INTERFACE INFORMATION' for N & M) Hi time >=1 CLKI Lo time >=3 CLKI (NSRx>1) Lo time >=1 CLKI (NSRx=1)
WR	Chip select Write	1	Active hi, enables the internal data write logic. Must be synchronous to the rising or falling edge of the CLKI input. Data latches internally at the first rising edge of CLKI after WR goes Hi. Hi and Lo time for WR>=1 CLKI
DIN	Data In	DBW	Input Data Bus. Used only when EBUS=0, when EBUS=1, DOUT used for data input
CLKEN	Clock enable	1	Periodic pulses of 1 CLKI width and frequency of CEF. If unused connect to '1'
CNTEN	Count enable	1	When Hi, enables the Date and Time counters. Make Lo while loading data.

## OUTPUT PORTS

NAME	DESC	WIDTH	COMMENTS
DOUT	Data out/input	DBW	TRI-STATE buffers are enabled and data appears on it while RD is hi. Also used for Data input when EBUS=1
CSOR	Cascade out Read	1	Used in a cascaded configuration, to enable the next core in the chain for data loading from the data bus. When unused drives out Lo
CSOW	Cascade out Write	1	Used in a cascaded configuration, to enable the next core in the chain for data loading from the data bus. When unused drives out Lo
INTR	Interrupt	1	Periodic pulses with period of 1 sec and hi time of 1 CLKI period

## PARAMETERS-all INTEGER type

NAME	MIN	DESCRIPTION
RTC	1	Reserved. Leave 1 or unused
DBW	1	Width of DIN input port and DOUT output port . See "INTERFACE INFORMATION" above
LYR	0	Last Year eg 100 for year 2100
EBUS	0	DOUT port is taken out of chip, onto PCB – Yes (1), No (0). When EBUS=1, DIN is unused, DOUT is bi-directional, used for data input and output When EBUS=0, DIN is used for data input, DOUT is used for data output
CSCR	0	Core is cascaded – Yes (1), No (0). When CSCR=0, MSTR and CSIR inputs are unused and may be connected to '0', the CSOR output is always '0'.
CSCW	0	Core is cascaded – Yes (1), No (0). When CSCW=0, MSTW and CSIW inputs are unused and may be connected to '0', the CSOW output is always '0'.
GCL	0	Frequency of CLKI input. GCL>=5 KHz
CEF	0	Frequency of CLKEN input. CEF=0 if CLKEN='1', else CEF>=1 Hz