



P_ARITY

DESCRIPTION

Parity checker. Counts the number of '1' bits in the input bus. If this number is odd, the PRTY output is '1' otherwise it is '0'.

VHDL Component Declaration:

```
COMPONENT P_ARITY
  GENERIC(
    WD      : INTEGER := 1
  );
  PORT(
    IP      : IN  BUS1D(WD DOWNT0 0) := '0';
    PRTY    : BUFFER NODE
  );
END COMPONENT;
```

FILES YOU GET

- i) FUNC.DOC - Documentation of functions & data types used in the core.
- ii) README.DOC - Compile and licensing information.
- iii) PARITY.DOC - This document

- a) MYLIB.VHD - PACKAGE
- b) P_ARITY.VHD - TOP HIERARCHY DESIGN FILE

INPUT PORTS

Port Name	Required	Description	Comments
IP	Yes	Data input	Input port WD+1 bits wide-

OUTPUT PORTS

Port Name	Required	Description	Comments
PRTY	Yes	Data output	1 bit wide. The result of parity checking on input port IP[]

PARAMETERS

Parameter	Type	Required	Description
WD	INTEGER	No	Bit Width-1 of input bus. Default is 1



SAMPLE DESIGN

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
  PORT(IP      :IN  BUS1D(DOWNT0 0);
        PRTY   :BUFFER NODE
        );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

BEGIN

A1: P_ARITY GENERIC MAP (W=>7) PORT MAP (IP,PRTY);

END MYTOP;
```

