



D LATCH ARRAY

DESCRIPTION

The M_LCH.VHD ipcore described here is an array of transparent latches, with user specified width. All the flip-flops share a common clock and asynchronous load, reset, preset and enable signals and individual 'D' inputs.

VHDL Component Declaration:

```
COMPONENT M_LCH
  GENERIC(
    W      : INTEGER:=0
  );
  PORT(
    D      : IN  BUS1D(W DOWNT0 0) := '0';
    ENB    : IN  NODE:= '1';
    CLR    : IN  NODE:= '1';
    PRN    : IN  NODE:= '1';
    Q      : BUFFER BUS1D(W DOWNT0 0);
  );
END COMPONENT;
```

FILES YOU GET

- i) FUNC.DOC - Documentation of functions & data types used in the core.
- ii) README.DOC - Compile and licensing information.
- iii) MLCH.DOC - This document

- a) MYLIB.VHD - PACKAGE
- b) M_LCH.VHD - TOP HIERARCHY DESIGN FILE
- c) S_LCH.VHD - DESIGN FILE BELOW TOP HIERARCHY

INPUT PORTS

Name	Required	Description	Comment
D	No	Data input to latches	Input port W+1 bits wide. If unused, PRN or CLR must be used.
ENB	Yes	Latch enable input. High=flow-through, Low=latch.	
CLR	No	Asynchronous clear	Active lo, default=1. Sets the latch to all 0's If PRN and CLR are used and both are asserted, CLR is dominantA
PRN	No	Asynchronous preset	Active lo, default=1. Sets latches to all 1's If PRN and CLR are used and both are asserted, CLR is dominantA

OUTPUT PORTS

Name	Required	Description	Comments
Q	Yes	Data output from the latch	W+1 bits wide.



PARAMETERS

Namer	Type	Required	Description
W	INTEGER	No	Width, When not specified, 1 S LCH is instantiated

FUNCTION

CLR	PRN	ENB	Q[W..0]
L	X	X	000...
H	L	X	111...
L	L	X	000...
H	H	L	Q[] (no change)
H	H	H	D[\Rightarrow]Q[]

SAMPLE DESIGN

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
  PORT(ENB      :IN  NODE;
        CLR     :IN  NODE;
        PRN     :IN  NODE;
        D       :IN  BUS1D(15 DOWNT0 0);
        Q       :BUFFER BUS1D(15 DOWNT0 0)
  );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

BEGIN

A1: M_LCH GENERIC MAP (W=>15) PORT MAP (D,ENB,CLR,PRN,Q);

END MYTOP;
```