



JK FLIP-FLOP ARRAY

DESCRIPTION

The M_JKF.VHD ipcore described here is an array of JK flip-flops, with user specified width. All the flip-flops share a common clock and asynchronous load, reset, preset and enable signals and individual 'J' and 'K' inputs.

VHDL Component Declaration:

```
COMPONENT M_JKF
  GENERIC (
    W      : INTEGER := 0
  );
  PORT (
    J      : IN  BUS1D(W DOWNTO 0) := '0';
    K      : IN  BUS1D(W DOWNTO 0) := '0';
    CLKI   : IN  NODE := '1';
    CLR    : IN  NODE := '1';
    PRN    : IN  NODE := '1';
    ENB    : IN  NODE := '1';
    Q      : BUFFER BUS1D(W DOWNTO 0);
  );
END COMPONENT;
```

FILES YOU GET

- i) FUNC.DOC - Documentation of functions & data types used in the core.
- ii) README.DOC - Compile and licensing information.
- iii) MJKF.DOC - This document

- a) MYLIB.VHD - PACKAGE
- b) M_JKF.VHD - TOP HIERARCHY DESIGN FILE
- c) S_JKF.VHD - DESIGN FILE BELOW TOP HIERARCHY
- d) S_DFF.VHD - -do-

INPUT PORTS

Port Name	Required	Description
J	Yes	J input to flipflopS, W+1 bits wide-
K	Yes	K input to flipflops, W+1 bits wide-
CLKI	Yes	Positive edge triggered clock.
CLR	No	Clear, active low,clears flipflops to low.
PRN	No	Preset, active low, presets flipflops to hi
ENB	No	Clock enable, output remains frozen when low.

OUTPUT PORTS

Port Name	Required	Description	Comments
Q	Yes	Data output from flipflops	W+1 bits wide.

PARAMETERS

Parameter	Type	Required	Description
W	INTEGER	No	Width, When not specified, 1 S_JKF is instantiated



FUNCTION

J[W..0]	K[W..0]	CLR	CLKI	PRN	ENB	Q[W..0]
X	X	L	X	X	X	L
X	X	H	X	L	X	H
X	X	L	X	L	X	illegal
X	X	H	X	H	L	Q (no change)
H	L	H	↑	H	H	H
L	H	H	↑	H	H	L
H	H	H	↑	H	H	Toggle
L	L	H	X	H	H	Q (no change)

SAMPLE DESIGN

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
  PORT(CLKI :IN NODE;
        CLR :IN NODE;
        PRN :IN NODE;
        J :IN BUS1D(15 DOWNTO 0);
        K :IN BUS1D(15 DOWNTO 0);
        Q :BUFFER BUS1D(15 DOWNTO 0)
  );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

BEGIN

A1: M_JKF GENERIC MAP (W=>15) PORT MAP (J,K,CLKI,CLR,PRN,ENB,Q);

END MYTOP;
```