



D FLIP-FLOP ARRAY

DESCRIPTION

The M_DFF.VHD ipcore described here is an array of D flip-flops, with user specified width. All the flip-flops share a common clock and asynchronous load, reset, preset and enable signals and individual 'D' inputs.

VHDL Component Declaration:

```
COMPONENT M_DFF
  GENERIC(
    W      : INTEGER:=0;
    L      : INTEGER:=0
  );
  PORT(
    D      : IN  BUS1D(W-1 DOWNT0 0):= '0';
    CLKI   : IN  NODE:= '1';
    CLR    : IN  NODE:= '1';
    PRN    : IN  NODE:= '1';
    ENB    : IN  NODE:= '1';
    Q      : BUFFER BUS1D(W-1 DOWNT0 0);
  );
END COMPONENT;
```

FILES YOU GET

- i) FUNC.DOC - Documentation of functions & data types used in the core.
- ii) README.DOC - Compile and licensing information.
- iii) M_DFF.DOC - This document

- a) MYLIB.VHD - PACKAGE
- b) M_DFF.VHD - TOP HIERARCHY DESIGN FILE
- c) S_DFF.VHD - DESIGN FILE BELOW TOP HIERARCHY

INPUT PORTS

Port Name	Required	Description	Comments
D	Yes	Data input to flipflops	Input port W bits wide-
CLKI	Yes	Positive edge triggered clock	Q[] output changes to D[] at rising edge
CLR	No	Asynchronous clear / load	Active lo, when L>0 will load flipflops with L
PRN	No	Asynchronous preset	Active lo, presets flipflops to hi
ENB	No	Clock enable	Output remains frozen when low

OUTPUT PORTS

Name	Required	Description	Comments
Q	Yes	Data output from flipflops	W bits wide.

PARAMETERS

Name	Type	Required	Description
W	INTEGER	No	Width, When not specified, 1 DFF is instantiated
L	INTEGER	Yes	Asynchronous load value, when not specified, CLR=0 will reset Q. When L>0, CLR=0 will load L to Q



FUNCTION

CLR	CLKI	PRN	ENB	Q[W..0]
L	X	X	X	000... or L (if L>0)
H	X	L	X	111...
L	X	L	X	illegal
H	X	H	L	Q[] (no change)
H	↑	H	H	D[]=>Q[]

SAMPLE DESIGN

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
  PORT(CLKI :IN NODE;
        CLR  :IN NODE;
        PRN  :IN NODE;
        D    :IN BUS1D(15 DOWNT0 0);
        Q    :BUFFER BUS1D(15 DOWNT0 0)
  );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

BEGIN

A1: M_DFF GENERIC MAP (W=>16,L=>10) PORT MAP (D,CLKI,CLR,PRN,ENB,Q);

END MYTOP;
```