



# FREQUENCY DIVIDER

## DESCRIPTION

The F\_DIV.VHD ipcore described here is a Generic Frequency divider. It generates frequency divided square wave and clock enable outputs.

## VHDL Component Declaration:

```
COMPONENT F_DIV
  GENERIC(
    CNT      : INTEGER := 1
  );
  PORT(
    CLKI     : IN  NODE;
    RST      : IN  NODE := '1';
    ENB      : IN  NODE := '1';
    OCL      : BUFFER BUS1D(3 DOWNT0 0);
    AA       : BUFFER BUS1D(LOG2(CNT-1) DOWNT0 0)
  );
END COMPONENT;
```

## FILES YOU GET

- i) FUNC.DOC - Documentation of functions & data types used in the core.
- ii) README.DOC - Compile and licensing information.
- iii) FDIV.DOC - This document
  
- a) MYLIB.VHD - PACKAGE
- b) F\_DIV.VHD - TOP HIERARCHY DESIGN FILE
- c) M\_DFF.VHD - DESIGN FILE BELOW TOP HIERARCHY
- d) S\_DFF.VHD - -do-
- e) U\_DCNT.VHD - -do-
- f) S\_JKF.VHD - -do-
- g) S\_TFF.VHD - -do-
- h) I\_NCDEC.VHD - -do-
- i) A\_DSB.VHD - -do-

## INPUT PORTS

Port Name	Required	Description	Comments
CLKI	Yes	clock	Synchronizes all internal operations
RST	No	reset	Resets all internal registers
ENB	No	clock enable	Enable all internal registers

## OUTPUT PORTS

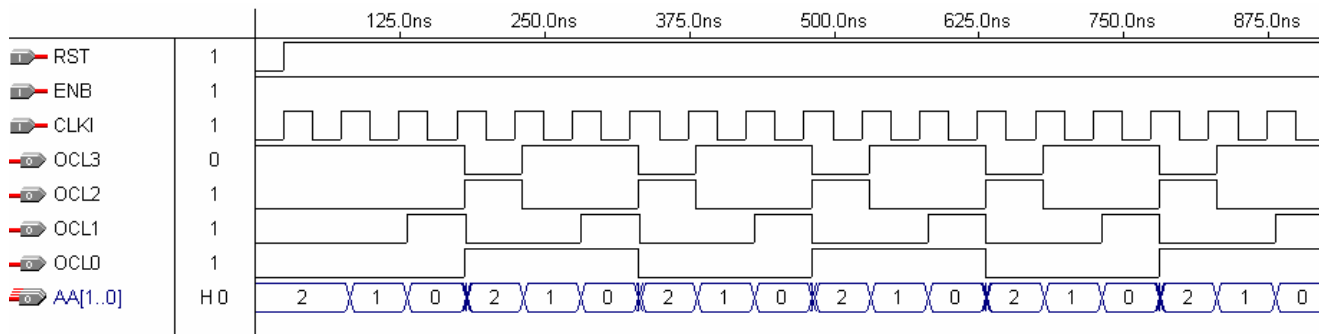
Port Name	Description	Comments
AA[log2(CNT-1)..0]	Count	Width: log2(CNT-1)+1 bits.
OCL(0)	Square wave o/p	Width: 1 bit
OCL(1)	Terminal count	Can be used as clock enable
OCL(2)	OCL[1] registered.	Width: 1 bit
OCL(3)	OCL[2] inverted.	Width: 1 bit



## PARAMETERS

Parameter	Type	Required	Description
CNT	INTEGER	No	Terminal count When frequency of OCL[1] is specified $CNT = \lceil \text{freq CLKI} / \text{freq OCL}(1) \rceil$ When frequency of OCL[0] is specified $CNT = \lceil \text{freq CLKI} / 2 * \text{freq OCL}(0) \rceil$

## TIMING DIAGRAM – CNT=2

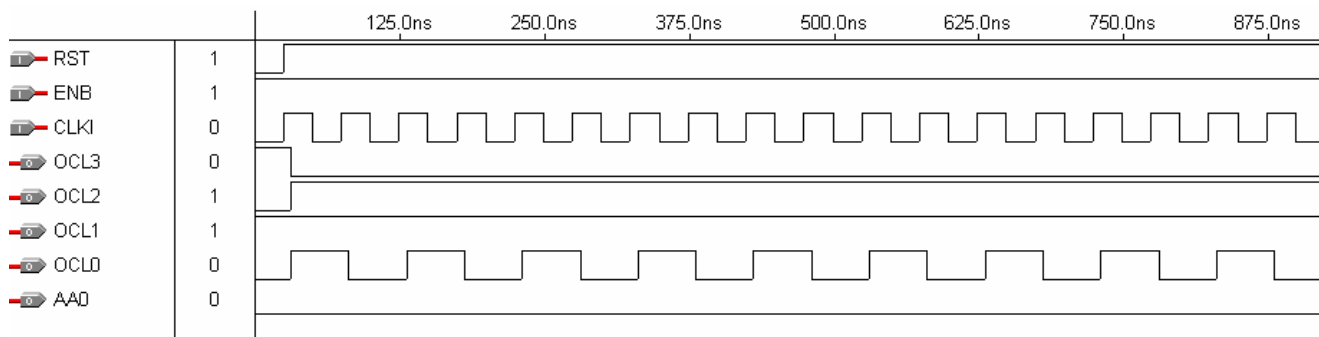


## FUNCTION – CNT>0

Inputs			Outputs				
Clki	rst	enb	ocl[0]	ocl[1]	ocl[2]	ocl[3]	aa[log2(CNT-1)..0]
X	0	X	0	0	0	1	CNT
X	1	0	ocl[0]	0	ocl[2]	ocl[3]	aa[]
↑	1	1	ocl[1] & !ocl[0]	aa[]==1	ocl[1]	!ocl[1]	aa[]-1

Note: Last row signals appear at o/p on rising edge of CLKI. “a[]==1” means ocl[1]=1 if aa[]==1 else ocl[1]=0

## TIMING DIAGRAM – CNT=1





## SAMPLE DESIGN

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
  PORT(CLKI   :IN  NODE;
        RST   :IN  NODE:= '1';
        ENB   :IN  NODE:= '1';
        OCL   :BUFFER BUS1D(3 DOWNT0 0);
        AA    :BUFFER BUS1D(1 DOWNT0 0)
        );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS

BEGIN

A1: F_DIV GENERIC MAP (CNT=>3) PORT MAP (CLKI,RST,ENB,OCL,AA);

END MYTOP;
```