



DEBOUNCE

DESCRIPTION

The D_X.VHD ipcore described here filters out variable frequency noise from digital inputs.

VHDL Component Declaration:

```
COMPONENT D_X
  GENERIC (
    CNY      : INTEGER := 0;
    S_IM     : INTEGER := 0;
    SC       : INTEGER := 0;
  );
  PORT (
    PRN      : IN  NODE := '1';
    G        : IN  NODE := '1';
    DCLK     : IN  NODE := '1';
    RST      : IN  NODE := '1';
    ENB      : IN  NODE := '1';
    GOUT     : BUFFER NODE;
  );
END COMPONENT;
```

FILES YOU GET

i) FUNC.DOC	-	Documentation of functions & data types used in the core.
ii) README.DOC	-	Compile and licensing information.
iii) DX.DOC	-	This document
a) MYLIB.VHD	-	PACKAGE
b) D_X.VHD	-	TOP HIERARCHY DESIGN FILE
c) R_SL.VHD	-	DESIGN FILE BELOW TOP HIERARCHY
d) S_JKF.VHD	-	-do-
e) S_DFF.VHD	-	-do-
f) F_DIV.VHD	-	-do-
g) S_TFF.VHD	-	-do-
h) U_DCNT.VHD	-	-do-
i) I_NCDEC.VHD	-	-do-
j) A_DSB.VHD	-	-do-
k) P_AD.VHD	-	-do-

INPUT PORTS

Port Name	Required	Description
G	Yes	Signal to be filtered, max frequency = freq of DCLK / (4 * CNY). Higher frequencies are considered noise and filtered out.
DCLK	Yes	Positive edge triggered clock to synchronize all operations.
RST	No	Asynchronous clear, active low, clears output to low.
PRN	No	Asynchronous preset, active low, sets output to hi
ENB	No	Clock enable, output remains frozen when low.

OUTPUT PORTS

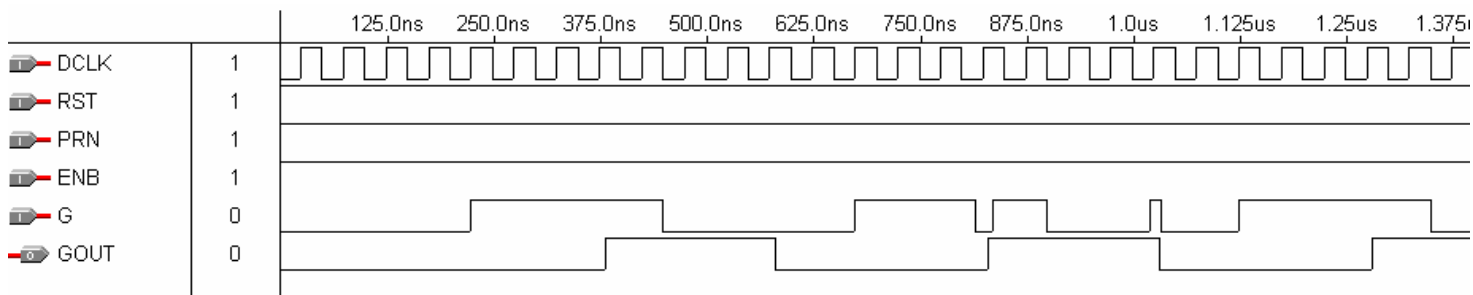
Port Name	Required	Description
GOUT	Yes	Filtered output



PARAMETERS

Parameter	Type	Required	Description
CNY	INTEGER	Yes	Filter count. When CNY=0, G input shorted to GOUT
S_IM	INTEGER	No	Must be 0 or unused.
SC	INTEGER	No	Must be 0 or unused.

TIMING DIAGRAM – CNY=1, S_IM=0, SC=0



SAMPLE DESIGN

```
LIBRARY IEEE;  
USE IEEE.STD_LOGIC_1164.ALL;  
USE IEEE.STD_LOGIC_ARITH.ALL;  
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
```

```
LIBRARY MYLIB;  
USE MYLIB.MYLIB.ALL;
```

```
ENTITY MYTOP IS  
    PORT(DCLK      :IN  NODE;  
         RST       :IN  NODE;  
         ENB       :IN  NODE;  
         G         :IN  NODE;  
         PRN       :IN  NODE;  
         GOUT      :BUFFER NODE
```

```
    );  
END MYTOP;
```

```
ARCHITECTURE MYTOP OF MYTOP IS
```

```
BEGIN
```

```
A1: D_X GENERIC MAP (CNY=>1)  
    PORT MAP (PRN, G, DCLK, RST, ENB, GOUT);
```

```
END MYTOP;
```