FPGA DESIGN OF A LED DISPLAY CONTROLLER

DESCRIPTION

The D_ISP.VHD IP core, described here is a design of an integrated circuit for an **LED DISPLAY controller**. The chip is designed in **VHDL** (Very High speed integrated Hardware Description Language) and is implemented on an **FPGA** (Field Programmable Gate Array)

, contains internal VRAM (video ram) amd CGROM (character graphic rom). Users send to the core, the modified ASCII code of the character to be displayed and the address of the LED module. This display data is sent for each module in the LED display. The core writes this information into the corresponding location in VRAM. The modified ASCII codes written to the VRAM correspond to addresses in the CGROM, which contains the bit map image for each character.The core scans the VRAM one location at a time, fetches the bit map image from the CGROM and outputs this on the LED pattern lines (PAT[]) along with the multiplexed module enable signal (MDL[]).

FEATURES

a)**Double buffered interface logic** allows configuration to any bus width**,** from **serial** to **parallel** of any width.
b)Interface using address and data bus, only data bus or port, **dedicated or shared.**
c)Instantiate the core as **stand-alone** or **cascaded**, in a daisy chain configuration.
d)**Daisy chain multiple cores** on **one port address**.
e)Configure any number of **LED modules** and any number of **segments per module**, with or without **decimal**.
f)**Programmable** display **ON/OFF** and module **blinking**.
g)Can be configured for **any oscillator frequency**
h)Internal **dual port VRAM** and **CGROM**

APPLICATION

Man machine interface on a host of instrumentation, control , data logger and consumer applications, hand held, portable and battery powered.

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VHDL Component Declaration:

```
COMPONENT D_ISP
      GENERIC (
            OREG  :INTEGER := 1;
            SEG   :STRING:="D:\MAX2VHDL\MYLIB\PKGM\TOY.MIF";
            DSP   :INTEGER := 1;
            CNY   :INTEGER := 8;
            CNZ   :INTEGER :=16;
            NCD   :INTEGER :=36;
            DCI   :INTEGER :=1;
            BLI   :INTEGER :=1;
            CEF   :INTEGER :=5000;
            OPN   :INTEGER :=0;
            ABW   :INTEGER :=20;
            DBW   :INTEGER :=10;
            CASC  :INTEGER :=0;
            GCL   :INTEGER :=20000000;
            EOPV  :INTEGER :=2;
            EOPA  :INTEGER :=2;
            DVC   :INTEGER :=2
      );
      PORT(
            CLKI  :IN   NODE;
            RST   :IN   NODE;
            ENB   :IN   NODE;
            XA    :IN   BUS1D(ABW-1 DOWNTO 0);
            D     :IN   BUS1D(DBW-1 DOWNTO 0);
            CS    :IN   NODE;
            CASI  :IN   NODE;
            MAST  :IN   NODE;
            MDL   :BUFFER BUS1D(CNY-1 DOWNTO 0);
            PAT   :BUFFER BUS1D(CNZ+DCI-1  DOWNTO 0);
            CASO  :BUFFER
      );
END COMPONENT;
```

FILES YOU GET

```
  i)FUNC.DOC     -     Documentation of functions & data types used in the core.
 ii)README.DOC   -     Compile and licensing information.
iii)DISP.DOC     -     This document
  a)MYLIB.VHD    -     PACKAGE
  b)D_ISP.VHD    -     TOP HIERARCHY DESIGN FILE
  c)M_DFF.VHD    -     DESIGN FILE BELOW TOP HIERARCHY
  d)S_DFF.VHD    -           -DO-
  e)P_AD.VHD     -           -DO-
  f)R_SL.VHD     -           -DO-
  g)I_NCDEC.VHD  -           -DO-
  h)U_DCNT.VHD   -           -DO-
  i)A_DSB.VHD    -           -DO-
  j)D_BIL.VHD    -           -DO-
  k)S_TFF.VHD    -           -DO-
  l)S_JKF.VHD    -           -DO-
  m)F_DIV.VHD    -           -DO-
  n)B_SHIFT.VHD  -           -DO-
  O)D_ECOD.VHD   -           -DO-
  p)P_LSE.VHD    -           -DO-
```


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COMPILE INFORMATION FOR QUARTUS (SPECIFIC)

1>Create an empty text file called "TOY.MIF" and copy paste the the contents given below into it.
2>Place TOY.MIF anywhere on your disk and make note of the path eg "D:\MAX2WORK\MYLIB\PKGM\TOY.MIF" and Equate the parameter "SEG" to this string.
3>The above file must be Saved with the following MS-WORD options
  a)Plain text file
  b)MS-DOS encoding and
  c)CR/LF at the end of every line.

THE CGROM FILE - CAHRACTER GRAPHIC ROM (TOY.MIF)

This file, the contents of which are given below, contains the bit map image of digits 0 to 9, characters "A" to "Z" and NULL. It thus contains 37 address locations. The ASCII code of characters "A" to "Z" is contiguous from 41h onwards, however it is stored in
TOY.MIF at location 01h onwards to 1Ah. ASCII code for numerals 0 to 9 is contiguous from 30h onwards, however it is stored in TOY.MIF at location 1Bh onwards. NULL is stored at location 00h. Thus:-

```
location in TOY.MIF for character data = ASCII-40h
location in TOY.MIF for numeric   data = ASCII-15h
```


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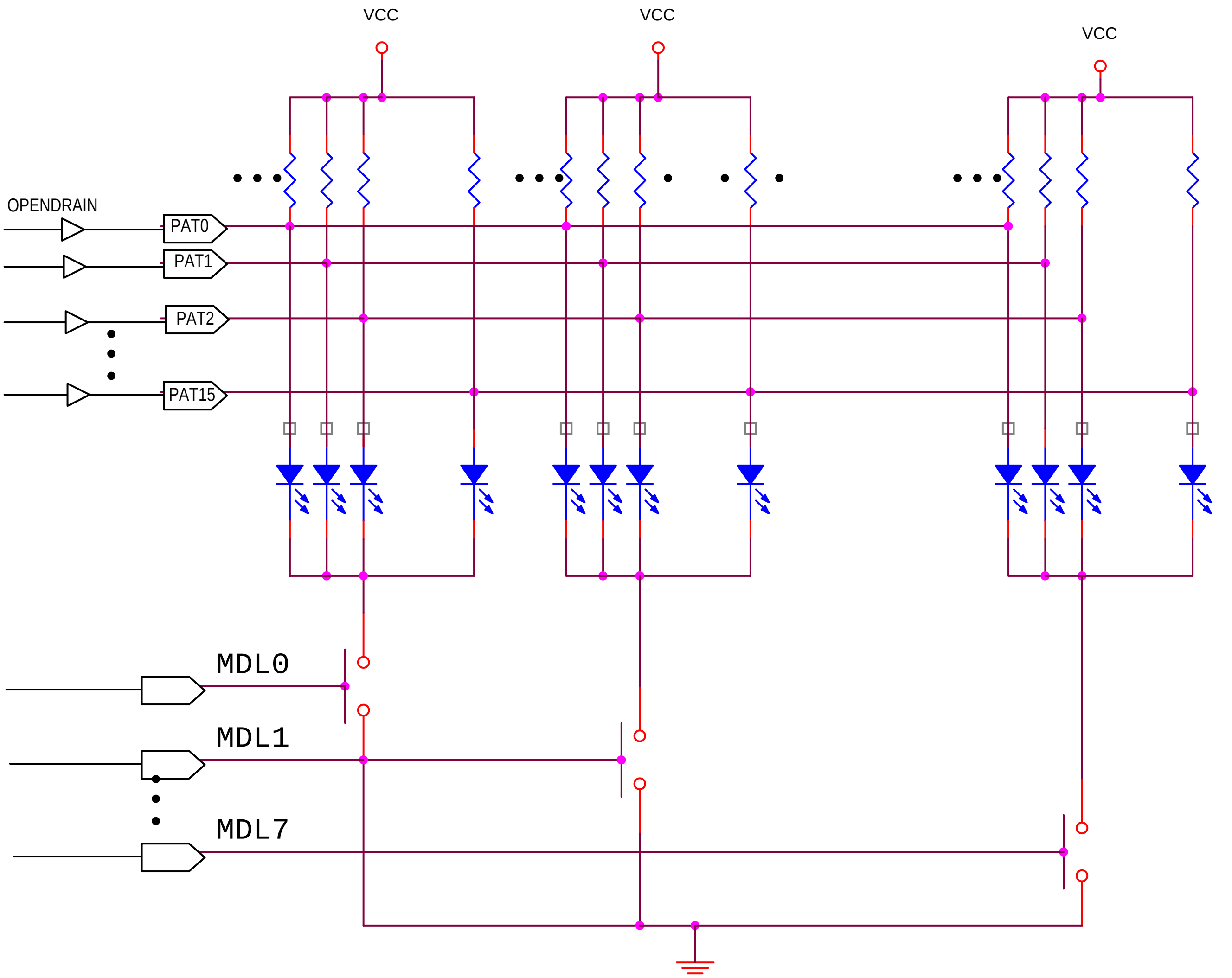
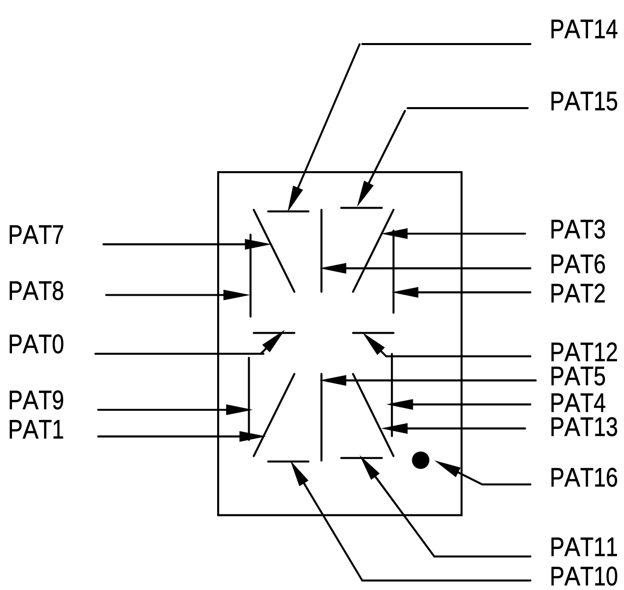
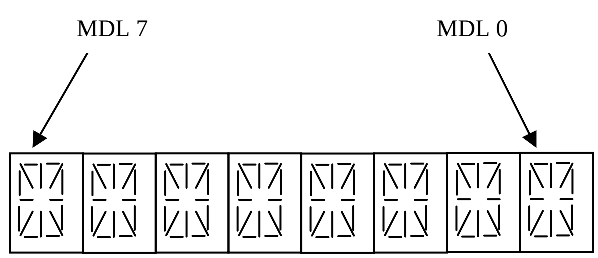
LED DISPLAY SCHEMATIC AND ARRANGEMENT







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INTERFACE INFORMATION

The interface schemes described here provide the user with information on how this core can be interfaced along with other peripherals on the common system resources, such as the address bus, data bus and output ports.

The three types of interface schemes are described here are:-

1) **Address and Data bus -** (**stand-alone** or **cascaded**)
2) **Data bus** (**stand-alone** or **Cascaded**)
3) **Port** (**stand-alone** or **Cascaded**)

In the first interface scheme the system address bus, data bus and a chip select (CS) line are used. VRAM address is sent on the address bus and CGROM address on the data bus. The address bus in this scheme must have a minimum width of log2(CNY-1)+1. Iin the other two schemes the address bus is not used, both VRAM address(sent first in the form of an address word) and CGROM address(sent later in the form of a data word) are sent on the data bus or port. In these two schemes the core receives the data and address words contiguously after which, it initializes the data load logic to the first word..

In all the interface schemes the number of data lines (bus or port) may vary from one bit serial to parallel of any number of bits.
The number of bits of data transmitted at a time depends on the number of data lines connected to the core. If the number of data lines connected is less than that required for a full parallel transmission, the internal data word and address word (scheme 2,3) is sliced to the size of the data lines. Sliced information must be sent contiguously (in the same cascade chain scan, in case of a cascaded interface) until the whole data word and address word (scheme 2 ,3) is assembled internally. Calculation of the number of slices of address word (NSA) and data word is (NSD) is shown below.

In all the interface schemes the data bus, address bus and port can be shared with any number of peripherals. However the Chip Select line (CS) must be unique for every core instantiated in the stand-alone scheme and common to all cascaded cores instantiated in the cascaded interface scheme. Chip-select signals can be generated either by an i/o address decoder, within the PLD(in the bus interface schemes) or from an output port on a micro-controller(in the port interface schemes).

CASCADED

In cascaded interface, although the chip select logic overhead is minimum, the cores cannot be accessed randomly and must be accessed sequentially one after the other and the entire sequence must be completed everytime, a process known as daisy chaining. The core, configured as the master will load first followed by the next in the chain. After a core receives its data, it pulses the CASO output, which being connected to the next core in the chain, enables it for data reception. After all the cores in the chain are loaded, the master is once again enabled. In the cascade interface scheme only one VRAM and CGROM address can be written to in one scan of the cascade chain.

Cascading is enabled by setting the CASC parameter to one and connecting the MAST input of the first core in the chain to ‘1’ and the CASO output of each core to the CASI input of the next core in the chain. The CASO output of the last core in the chain is connected to the CASI input of the master, or the first core in the chain.

STAND-ALONE

In stand-alone interface the core is ready to accept data soon after RST=1. The core with an active CS signal will accept data and only one core at a time must be activated. Separate chip selects for each core facilitates random access.

Stand-alone option is enabled by setting the CASC parameter to zero, the MAST and CASI inputs are not used and may be connected to any constant.

CS TIMING CONSTRAINTS (CASCADED SCHEMES)

a) Frequency of CS <= 1/3 of CLKI
b) Hi time of CS >= 1 CLKI
c) Lo time of CS >= 1 CLKI

CS TIMING CONSTRAINTS (STAND-ALONE SCHEMES)

a) The CS signal of the next stand-alone core may come back to back after the CS of the last slice of the previously selected core with no gap in between.
b) Hi time of CS >= 1 CLKI.

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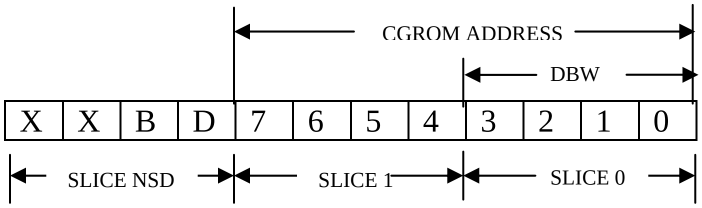
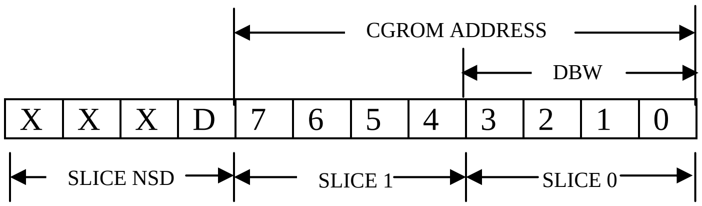
VRAM,ATTRIBUTE RAM DATA -DCI=1, BLI=1



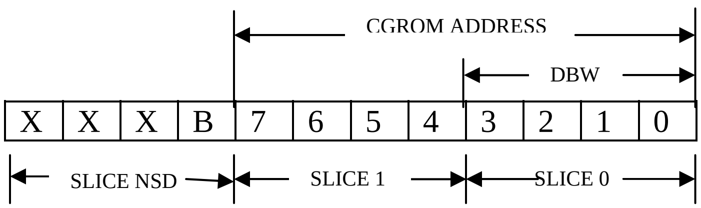
D-Decimal ON(1), OFF(0)
B-Blinking ON(1), OFF (0)

VRAM,ATTRIBUTE RAM DATA -DCI=1, BLI=0



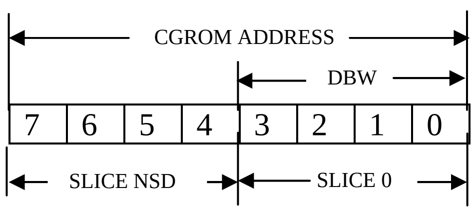
D-Decimal ON(1), OFF(0)

VRAM,ATTRIBUTE RAM DATA-DCI=0, BLI=1

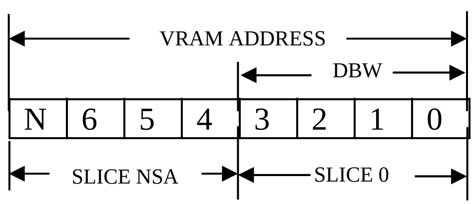


B-Blinking ON(1), OFF(0)

VRAM,ATTRIBUTE RAM DATA -DCI=0, BLI=0



VRAM,ATTRIBUTE RAM ADDRESS



N=log2(CNY-1)

CALCULATION OF NSD	**CALCULATION OF NSA**
NSD=[8+DCI+BLI] / DBW If the result of division produces a remainder, add 1 to result	OPN=1 : NSA=[Log2(CNY-1)+1] / DBW If the result of division produces a remainder, add 1 to result OPN=0 : NSA=Not applicable

VRAM	**ATTRIBUTE RAM**	**CGROM**
DPT=CNY --DEPTH WID=Log2(NCD-1)+1 --WIDTH	DPT=CNY --DEPTH WID=DCI+BLI --WIDTH	DPT=NCD --DEPTH WID=CNZ --WIDTH

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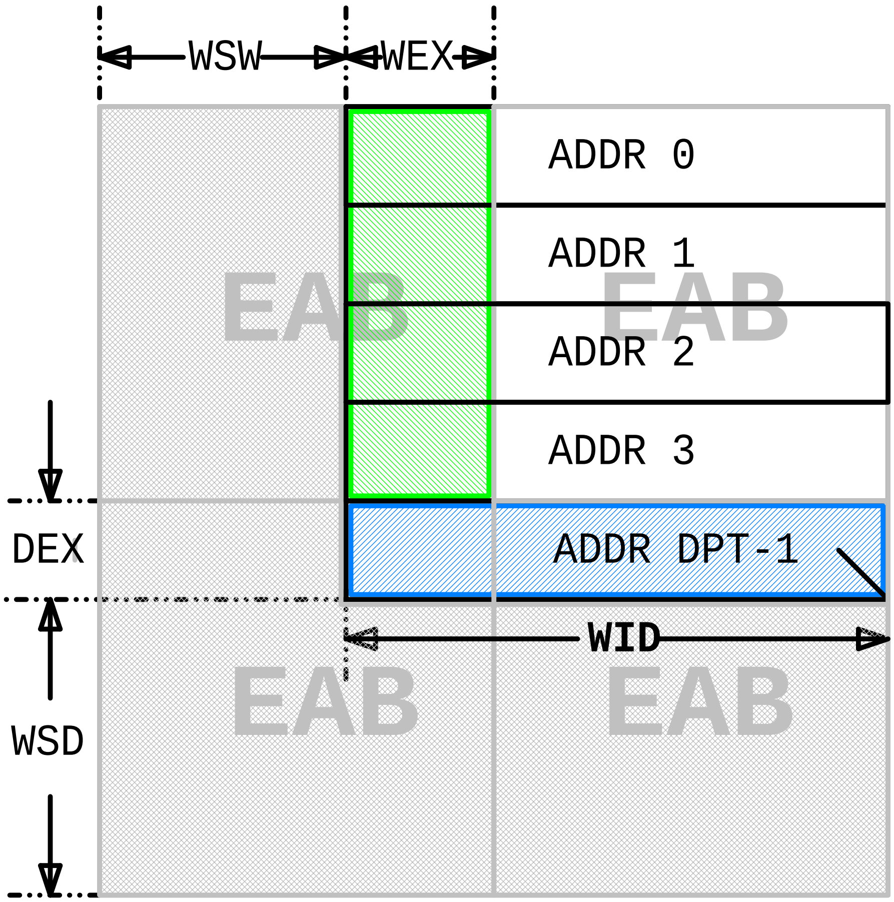
MEMORY STRUCTURE



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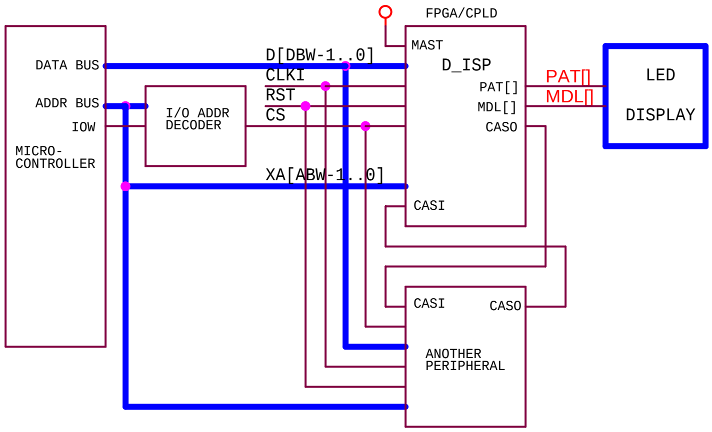
1-ADDRESS and DATA BUS - Set the OPN parameter to 0

1a-CASCADED – Set the CASC parameter to 1



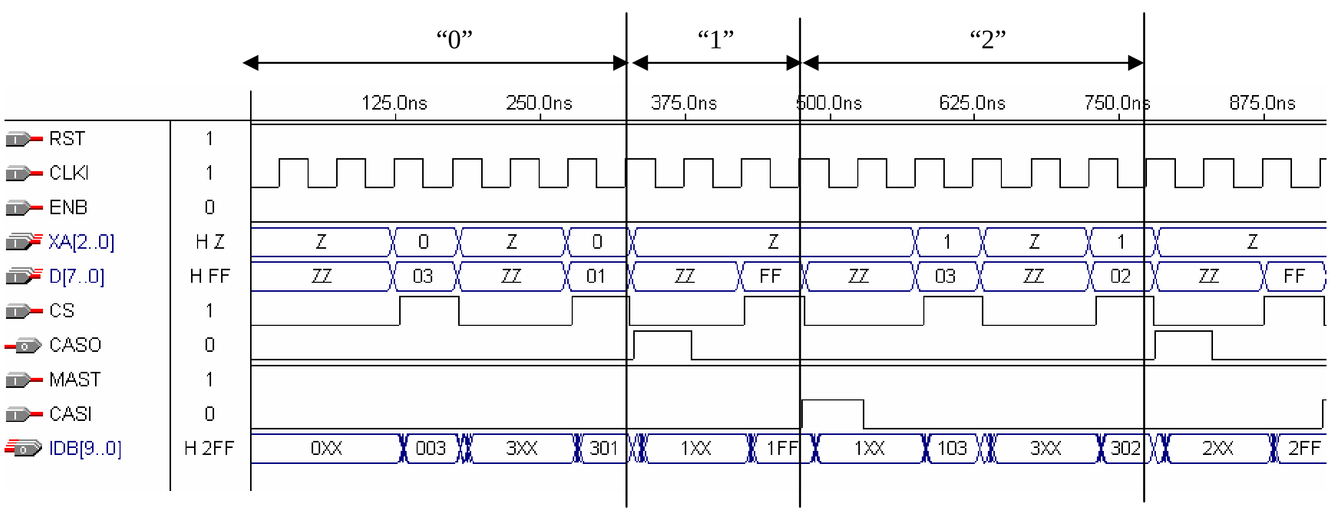
TIMING DIAGRAM

On a 3 bit address bus and 8 bit data bus we desire to do as follows:-

1)Send CGROM address 301H to VRAM address 0H - (section "0" in timing diagram)
2)Write data to cascaded peripheral - (section "1" in timing diagram)
3)Send CGROM address 302H to VRAM address 1H - (section "2" in timing diagram)

Parameter settings: OREG=1,SEG="D:\MAX2WORK\MYLIB\PKGP\TOY.MIF"
DSP=1,CNY=8,CNZ=16,NCD=36,DCI=1,BLI=1,CEF=0,
OPN=0,ABW=3,DBW=8,CASC=1,GCL=20000000

Slice calculations: NSD=[8+DCI+BLI] / DBW = 10/8=1+1=2
NSA=not applicable



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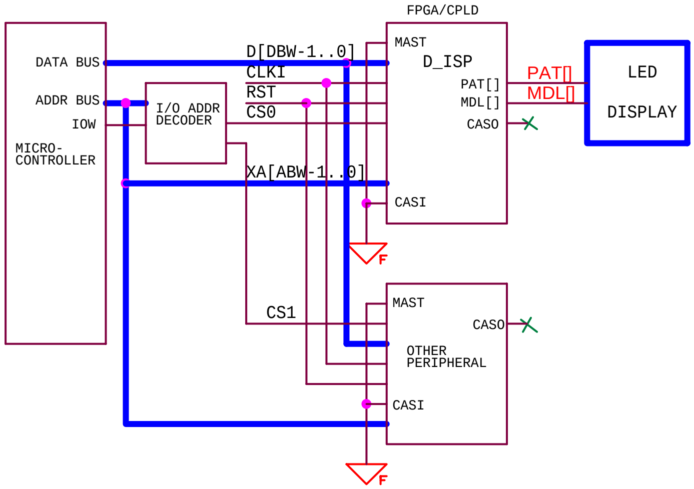
1b-STAND-ALONE– Set the CASC parameter to 0



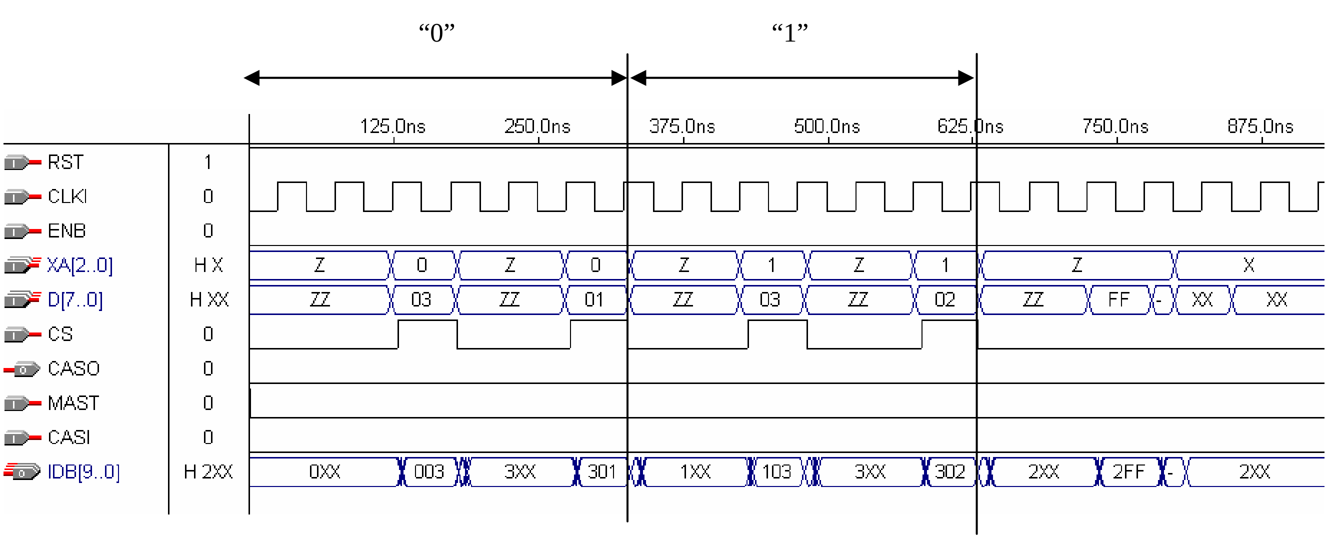
TIMING DIAGRAM

On a 3 bit address bus and 8 bit data bus we desire to do as follows:-

1)Send CGROM address 301H to VRAM address 0H - (section “0” in timing diagram)
3)Send CGROM address 302H to VRAM address 1H - (section “11” in timing diagram)

Parameter settings: OREG=1,SEG=”D:\MAX2WORK\MYLIB\PKGP\TOY.MIF”
DSP=1,CNY=8,CNZ=16,NCD=36,DCI=1,BLI=1,CEF=0,
OPN=0,ABW=3,DBW=8,CASC=0,GCL=20000000

Slice calculations: NSD=[8+DCI+BLI] / DBW = 10/8=1+1=2
NSA=not applicable



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2-DATA BUS - Set the OPN parameter to 1

2a-CASADED - Set the CASC parameter to 1

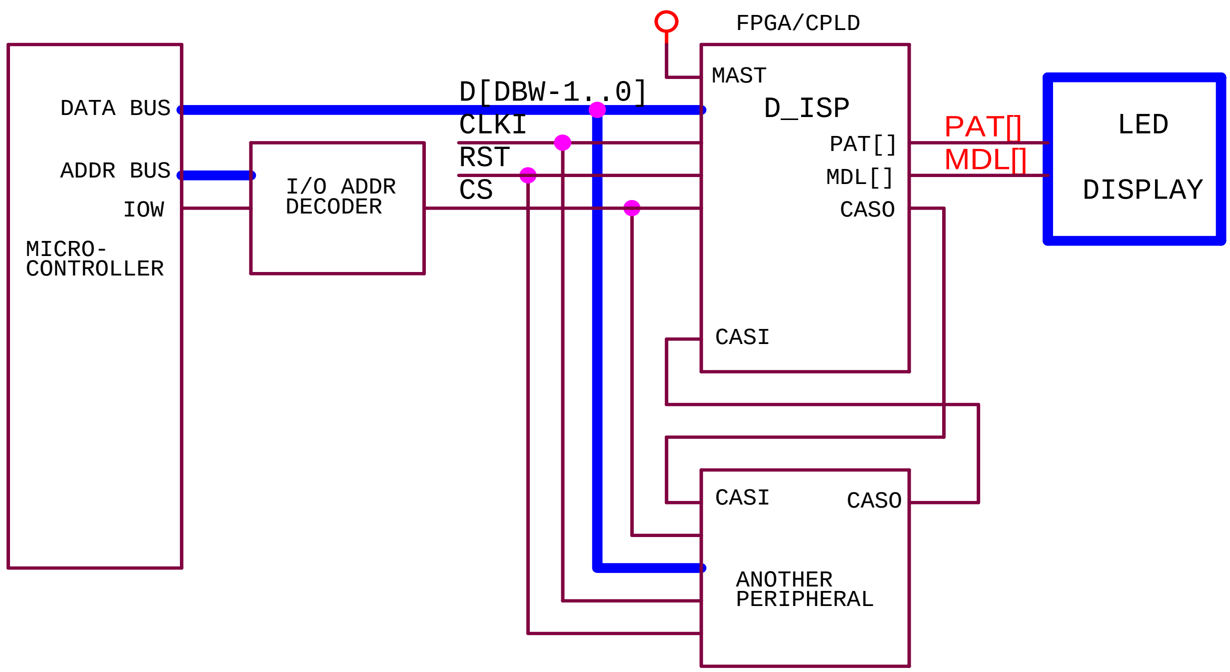
TIMING DIAGRAM

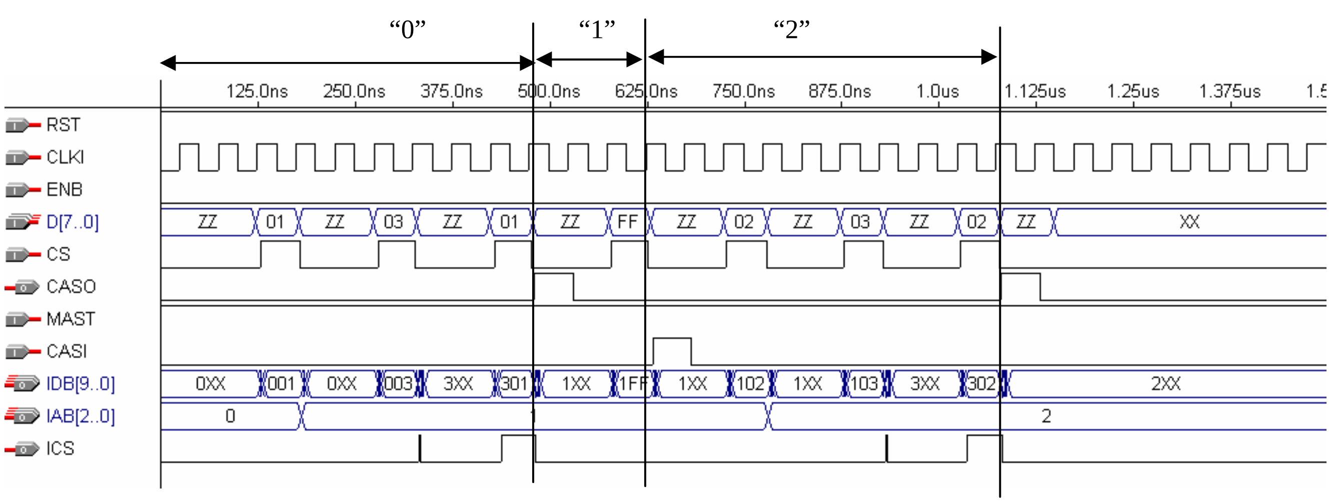
On a 3 bit address bus and 8 bit data bus we desire to do as follows:-

1)Send CGROM address 301H to VRAM address 1H - (section “0” in timing diagram)
2)Write data to cascaded peripheral - (section “1” in timing diagram)
3)Send CGROM address 302H to VRAM address 2H - (section “2” in timing diagram)

Parameter settings: OREG=1,SEG=”D:\MAX2WORK\MYLIB\PKGP\TOY.MIF”
DSP=1,CNY=8,CNZ=16,NCD=36,DCI=1,BLI=1,CEF=0,
OPN=1,ABW=1,DBW=8,CASC=1,GCL=20000000

Slice calculations: NSD=[8+DCI+BLI] / DBW = 10/8=1+1=2
NSA=[Log2(CNY-1)+1] / DBW =[log2(7)+1]/8 = 2+1/8 = 3/8=0+1=1





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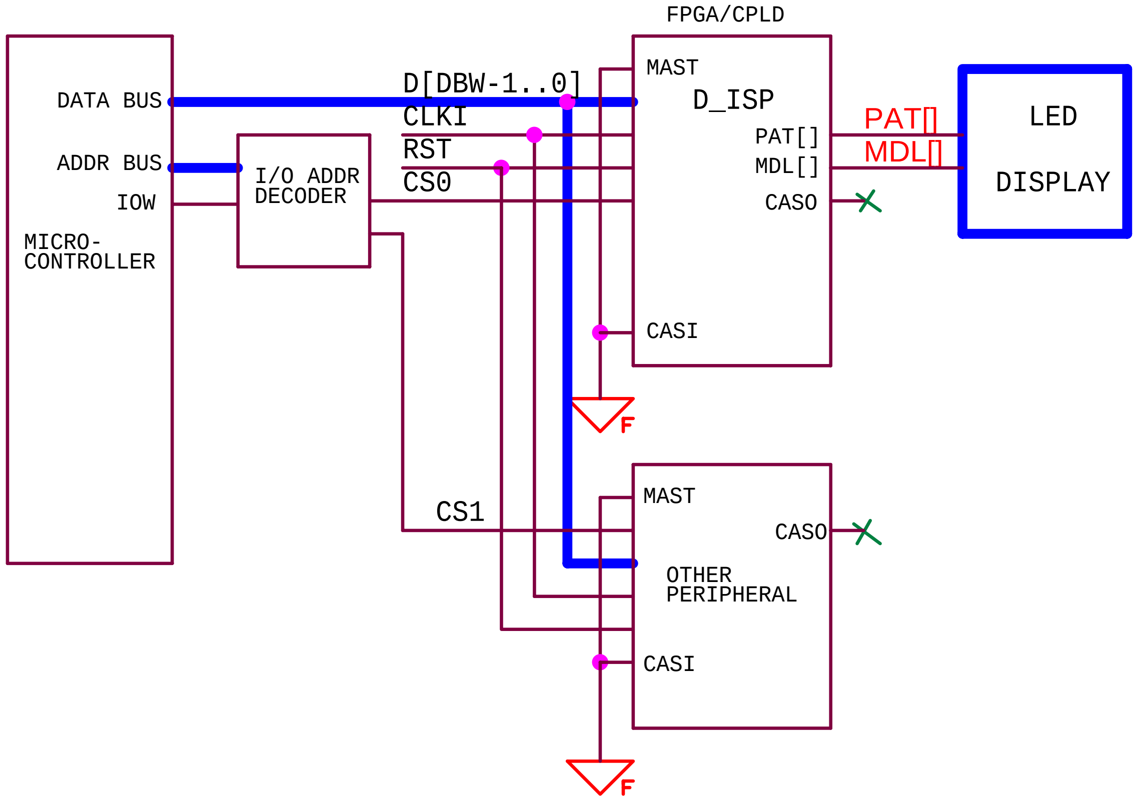
2b-STAND-ALONE - Set the CASC parameter to 0



TIMING DIAGRAM

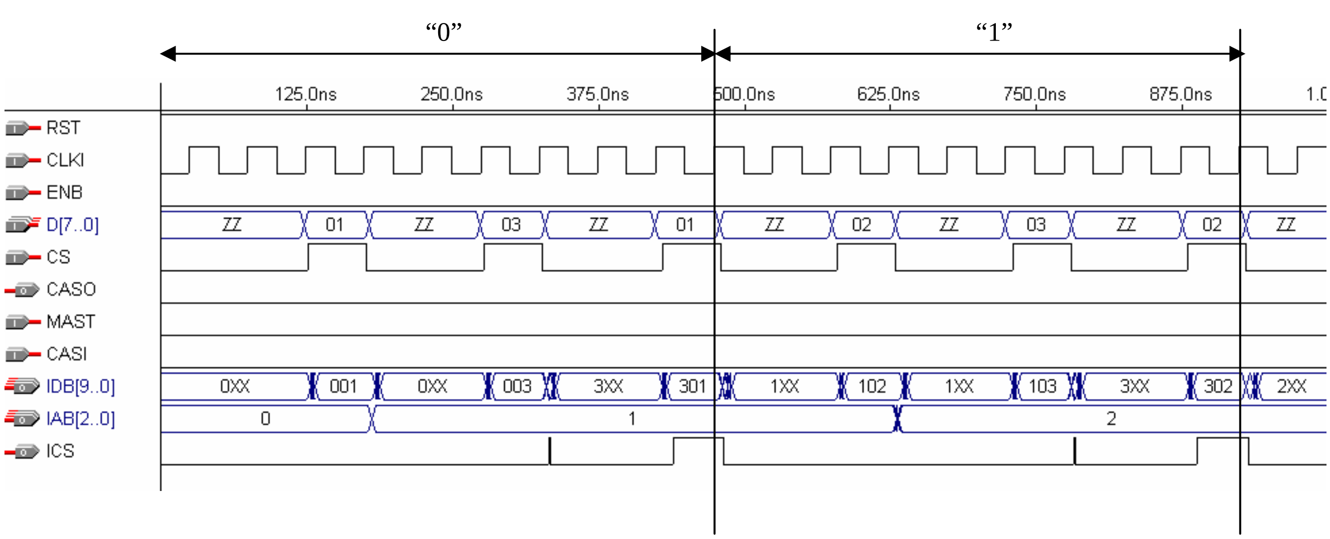
On a 3 bit address bus and 8 bit data bus we desire to do as follows:-

1)Send CGROM address 301H to VRAM address 1H - (section "0" in timing diagram)

2)Send CGROM address 302H to VRAM address 2H - (section "1" in timing diagram)

Parameter settings: OREG=1,SEG="D:\MAX2WORK\MYLIB\PKGP\TOY.MIF"
DSP=1,CNY=8,CNZ=16,NCD=36,DCI=1,BLI=1,CEF=0,
OPN=1,ABW=1,DBW=8,CASC=0,GCL=20000000

Slice calculations: NSD=[8+DCI+BLI] / DBW = 10/8=1+1=2
NSA=[Log2(CNY-1)+1] / DBW =[log2(7)+1]/8 = 2+1/8 = 3/8=0+1=1



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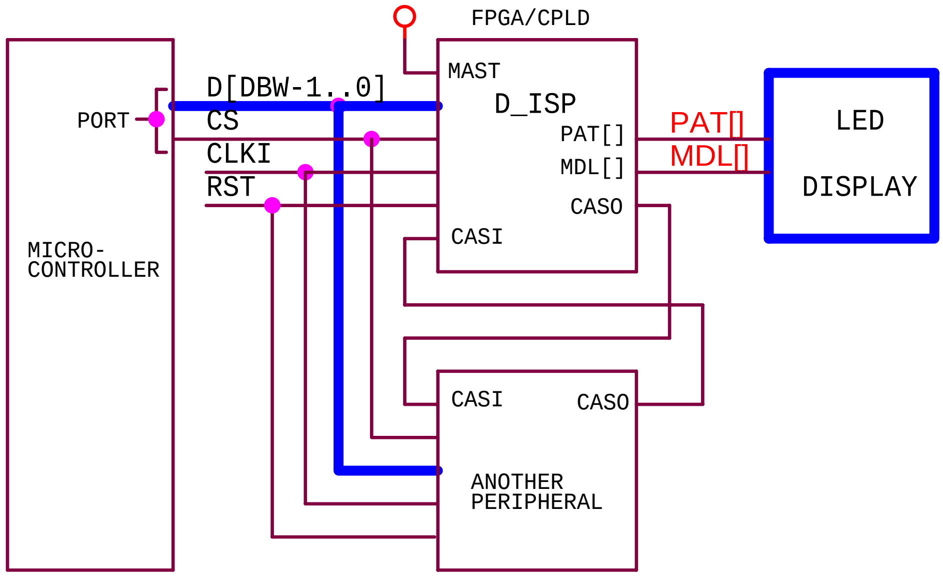
3-PORT - Set the OPN parameter to 1

3a-CASADED - Set the CASC parameter to 1

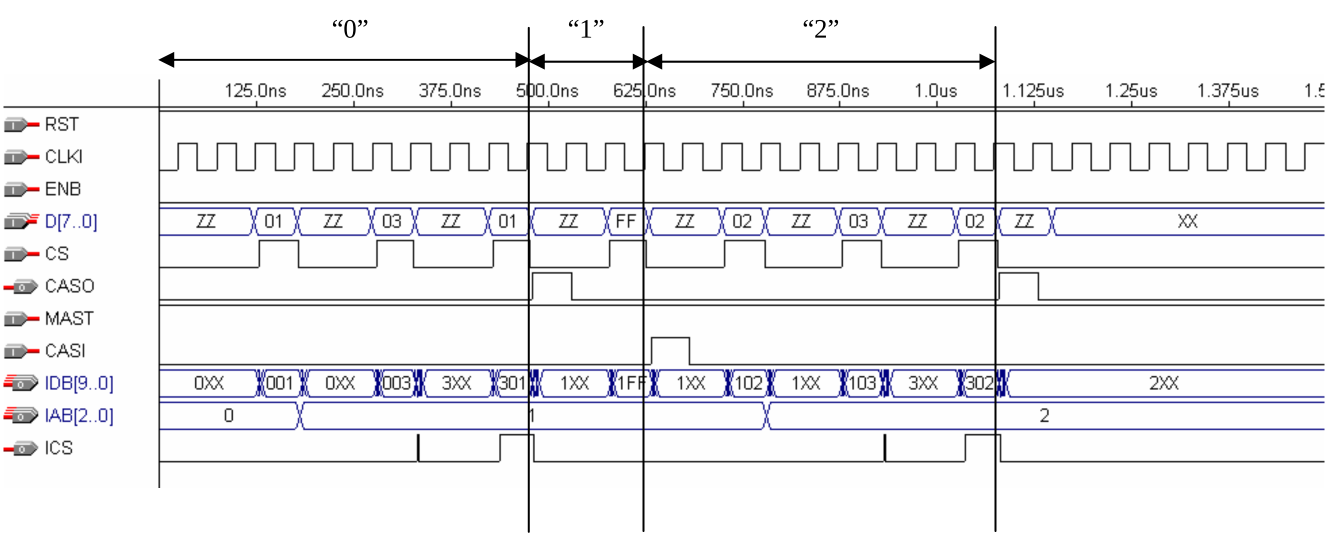


TIMING DIAGRAM
On a 3 bit address bus and 8 bit data bus we desire to do as follows:-

1)Send CGROM address 301H to VRAM address 1H - (section "0" in timing diagram)
2)Write data to cascaded peripheral - (section "1" in timing diagram)
3)Send CGROM address 302H to VRAM address 2H - (section "2" in timing diagram)

Parameter settings: OREG=1,SEG="D:\MAX2WORK\MYLIB\PKGP\TOY.MIF"
DSP=1,CNY=8,CNZ=16,NCD=36,DCI=1,BLI=1,CEF=0,
OPN=1,ABW=1,DBW=8,CASC=1,GCL=20000000

Slice calculations: NSD=[8+DCI+BLI] / DBW = 10/8=1+1=2
NSA=[Log2(CNY-1)+1] / DBW =[log2(7)+1]/8 = 2+1/8 = 3/8=0+1=1



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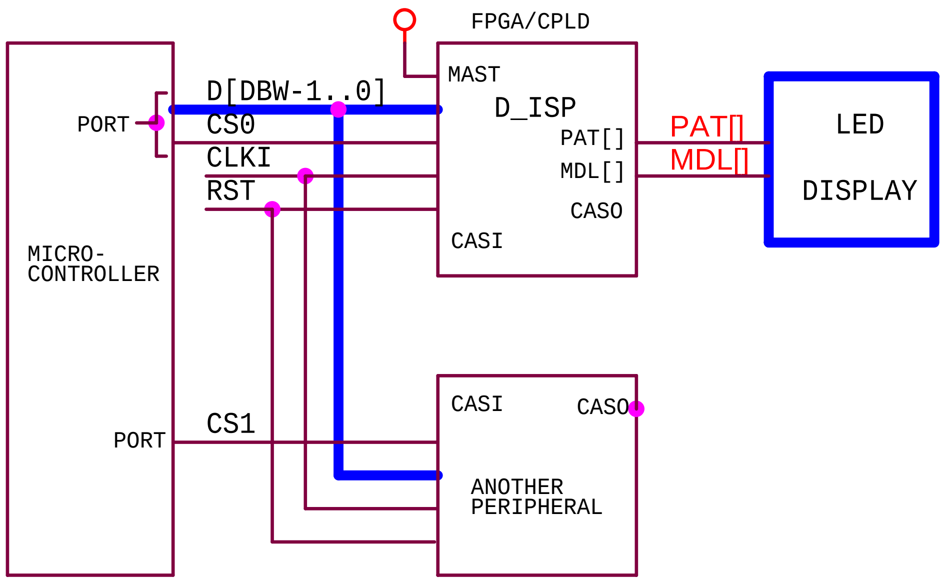
3b-STAND-ALONE - Set the CASC parameter to 0



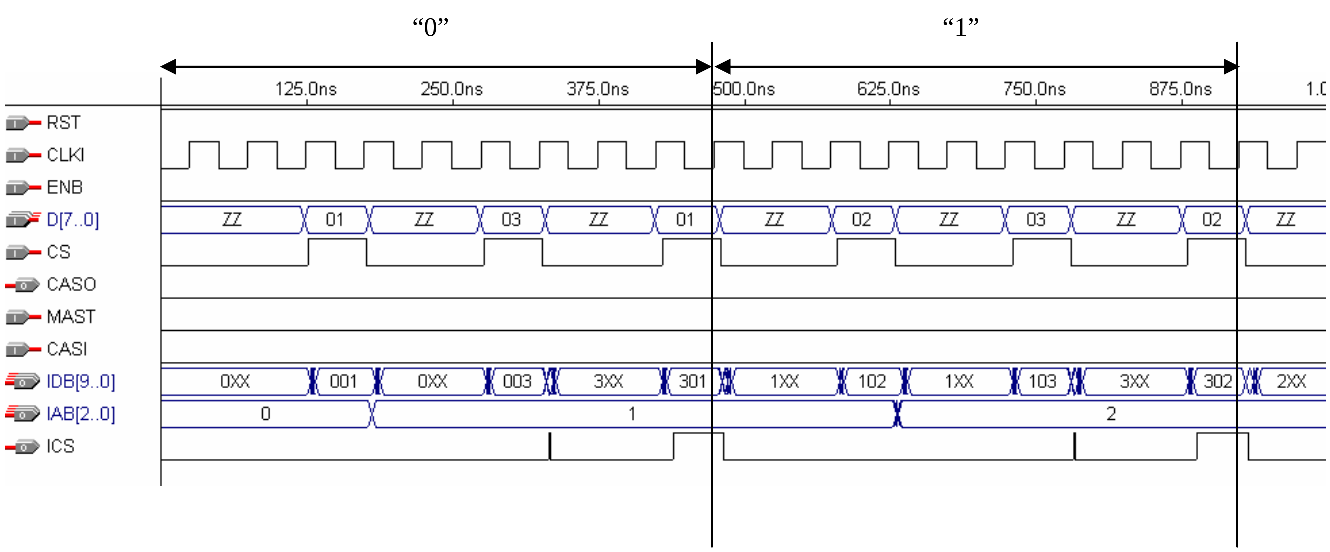
TIMING DIAGRAM

On a 3 bit address bus and 8 bit data bus we desire to do as follows:-

1)Send CGROM address 301H to VRAM address 1H - (section “0” in timing diagram)
3)Send CGROM address 302H to VRAM address 2H - (section “2” in timing diagram)

Parameter settings: OREG=1,SEG=”D:\MAX2WORK\MYLIB\PKGP\TOY.MIF”
DSP=1,CNY=8,CNZ=16,NCD=36,DCI=1,BLI=1,CEF=0,
OPN=0,ABW=3,DBW=8,CASC=1,GCL=20000000

Slice calculations: NSD=[8+DCI+BLI] / DBW = 10/8=1+1=2
NSA=[Log2(CNY-1)+1] / DBW =[log2(7)+1]/8 = 2+1/8 = 3/8=0+1=1



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INPUT PORTS

NAME	DESCRIPTION	WIDTH	COMMENTS
MAST	Master select	1	When the core is a master in a cascaded configuration and is the first core in the chain, set MAST to Hi. In a cascaded configuration if it is not the master, set it Lo. In a stand-alone Configuration, it is unused and may be left open.
CASI	Cascade in	1	In cascaded configuration the core is not the master connect CASI to CASO from the previos core in the chain, if it is the master, set it to CASO of the last core in the chain. Unused in stand-alone configuration and may be left open.
CLKI	Clock	1	Positive edge triggered. Synchronizes all internal operations
RST	Reset	1	Asynchronous, active lo, resets all internal logic
CS	Chip select	1	Active hi, enables the internal data load logic. Must be synchronous to the rising or falling edge of the CLKI input. Data latches internally at the first rising edge of CLKI after CS goes Hi. Only used when OPN<>0 See "**INTERFACE INFORMATION**" for timing constraints
D	Data bus	DBW	Data bus with VRAM data and address (when OPN=1) information
ENB	Clock enable	1	Periodic pulses of 1 CLKI width & frequency of CEF. If unused connect to '1'
XA	Address bus	ABW	Used only when OPN=0, else may be connected to any constant value

OUTPUT PORTS

NAME	DESCRIPTION	WIDTH	COMMENTS
MDL	Module Enable	CNY	Time division multiplexed signal to switch on the module transistor
PAT	LED pattern	CNZ+DCI	Signals for each line on an LED bus connected to all the Modules
CASO	Cascade out	1	In cascaded configuration enables the next core in the chain for loading data from the bus. Unused in stand-alone configuration and drives Lo.

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PARAMETERS(SEG is STRING Type, others INTEGER)

NAME	MIN	DESCRIPTION
OREG	0	PAT[]output is registered (1) , combinatorial (0)
SEG	-	Path and name of CGROM initialization file (see compile information)
DSP	1	Reserved. Leave 1 or unused
CNY	1	Number of LED modules
CNZ	1	Number of LED segments per module
NCD	0	Last address in CGROM
DCI	0	Decimal present and used (1), not present or not used (0)
BLI	0	Module blinking required – Yes (1) , No (0)
CEF	0	Frequency of ENB imput. CEF=0 if ENB='1', else CEF>=125*CNY
ABW	-	Address bus width. Unused when OPN=1. ABW >=(1-OPN)*Log2(CNY-1)+1
OPN	0	Bus interface option. See "INTERFACE INFORMATION" above
DBW	1	Data bus width. See "INTERFACE INFORMATION" above
CASC	0	Core is cascaded – Yes (1), No (0). When CASC=0, MAST and CASI inputs are unused, the CASO output is always '0'.
GCL	0	Frequency of CLKI input. GCL>=125*CNY
DVC	0	Device Family - CYCLONE(0),FLEX10K(1),ACEX(2)
EOPV	00	An integer array to optimize the VRAM Block. 1 digit wide X 2 digits deep. unused when OPN=0. Structure is :- (DR2,WR2) eg if DR2=2 & WR2=1, EOP=21. See table below.
EOPA	00	An integer array to optimize Attribute RAM Block. 1 digit wide X 2 digits deep. unused when OPN=0. Structure is :- (DR2,WR2) eg if DR2=2 & WR2=1, EOP=21. See table below.

ELEMENTS of EOPV,EOPA ARRAYS

WR2	Optimize memory block width to - LOWER(0),NEAREST(1),UPPER(2). If the slice width WID overflows into an adjacent memory block (Fig 5,6) the WEX and WSW bits of the block are used as follows(if part of depth is implemented in registers WR0,WR2 are ignored and WR2 is forced):- WR2=0 Adjacent horizontal EAB not used, WEX bits of width placed in registers WR2=1 When WEX>=WSW, WR2=2 is applied, otherwise WR2=0. WR2=2 Adjacent horizontal EAB used, WSW bits of EAB width are wasted and zero bits placed in registers.
DR2	Optimize memory block depth to - LOWER(0),NEAREST(1),UPPER(2). If the slice width WID overflows into an adjacent memory block (Fig 5,6) the DEX and WSD bits of the block are used as follows:- DR2=0 Adjacent vertical EAB not used, DEX bits of depth placed in registers DR2=1 When DEX>=WSD, DR2=2 is applied, otherwise DR2=0. DR2=2 Adjacent vertical EAB used, WSD bits of EAB depth are wasted and zero bits placed in registers..

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CONTENTS OF "TOY.MIF"- MEMORY FILE, FOR INTERNAL CGROM

```
WIDTH = 16;
DEPTH = 37;
ADDRESS_RADIX = HEX;
DATA_RADIX = HEX;

CONTENT BEGIN
      0     :     0000;       --NULL
      1     :     d315;       --A
      2     :     dc74;       --B
      3     :     cf00;       --C
      4     :     cc74;       --D
      5     :     df01;       --E
      6     :     d301;       --F
      7     :     df10;       --G
      8     :     1315;       --H
      9     :     cc60;       --I
      a     :     c660;       --J
      b     :     2309;       --K
      c     :     0f00;       --L
      d     :     039c;       --M
      e     :     2394;       --N
      f     :     cf14;       --O
      10    :     d305;       --P
      11    :     ef14;       --Q
      12    :     f305;       --R
      13    :     dd11;       --S
      14    :     c060;       --T
      15    :     0f14;       --U
      16    :     2094;       --V
      17    :     0f34;       --W
      18    :     208a;       --X
      19    :     00a8;       --Y
      1a    :     cc0a;       --Z
      1b    :     cf1e;       --0
      1c    :     0014;       --1
      1d    :     de05;       --2
      1e    :     dc15;       --3
      1f    :     1115;       --4
      20    :     dd11;       --5
      21    :     df11;       --6
      22    :     c014;       --7
      23    :     df15;       --8
      24    :     dd15;       --9
END;
```


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