

DOUBLE BUFFERED READ INTERFACE

DESCRIPTION

The D_BIR.VHD ipcore described here is a generic VHDL component for interfacing intellectual property megafunctions requiring data writing to a CPU data bus, for implementation in FPGA, ASIC and CPLD, VLSI devices.

FEATURES

- The data bus may be of any width, from a one bit serial to parallel of any width.
- The data to be loaded from the data bus may be of any width. If width is larger than the bus, data is disassembled into slices.
- May be cascaded to others within the mega function.
- Multiple megafunctions may be cascaded together on shared address, data and chip-select lines.
- A FIFO buffer maximizes throughput and can be implemented in memory or registers.
- Timing parameters enable it to be customised to any output constraints.
- Generates Chip-selects that enable CPU interfacing to synchronous/asynchronous memories & megafunctions.

VHDL Component Declaration:

```
COMPONENT D_BIR
GENERIC
    OPN          : INTEGER:=0;
    WR2          : INTEGER:=2;
    DR2          : INTEGER:=2;
    DVC          : INTEGER:=2;
    IWD          : INTEGER:=0;
    WSZ          : INTEGER:=0;
    BSW          : INTEGER:=0;
    SWD          : INTEGER:=0;
    ECAS        : INTEGER:=0;
    ICAS        : INTEGER:=0;
    FRST        : INTEGER:=0;
    QDI         : INTEGER:=0;
    QDE         : INTEGER:=0;
    IDV         : INTEGER:=0;
    RDEN        : INTEGER:=0;
    EBUS        : INTEGER:=0;
    CLTL        : INTEGER:=0;
    EXC         : INTEGER:=0;
PORT
    (
    D           : IN   BUS1D(IWD-1 DOWNTO 0) := (OTHERS=>'0');
    QI          : IN   BUS1D(BSW-1 DOWNTO 0) := (OTHERS=>'0');
    CLKI        : IN   NODE:='0';
    RST         : IN   NODE:='1';
    CS          : IN   NODE:='0';
    LDN         : IN   NODE:='0';
    MAST        : IN   NODE:='0';
    FSI         : IN   BUS1D(3 DOWNTO 0) := (OTHERS=>'0');
    CASI        : IN   BUS1D(3 DOWNTO 0) := (OTHERS=>'0');
    COM         : IN   BUS1D(3 DOWNTO 0) := (OTHERS=>'0');

    CASO        : BUFFER BUS1D(3 DOWNTO 0);
    QO          : BUFFER BUS1D(BSW-1 DOWNTO 0);
    OEN         : BUFFER NODE;
    FSO         : BUFFER BUS1D(3 DOWNTO 0);
    INTR        : BUFFER NODE;
    QR          : BUFFER NODE
    );END COMPONENT;
```

FILES YOU GET

i) FUNC.DOC	-	Documentation of functions & data types used in the core.
ii) README.DOC	-	Compile and licensing information.
iii) MDFD.DOC	-	This document
MYLIB.VHD	-	PACKAGE
S_TATE.VHD	-	TOP HIERARCHY DESIGN FILE
D_ECOD.VHD	-	DESIGN FILE BELOW TOP HIERARCHY
M_DFF.VHD	-	-do-
S_DFF.VHD	-	-do-
U_DCNT.VHD	-	-do-
S_JKF.VHD	-	-do-
S_TFF.VHD	-	-do-
I_NCDEC.VHD	-	-do-
A_DSB.VHD	-	-do-
F_DIV.VHD	-	-do-
P_LSE.VHD	-	-do-
B_SHIFT.VHD	-	-do-
R_STK.VHD	-	-do-
M_STK.VHD	-	-do-
F_IFO.VHD	-	-do-

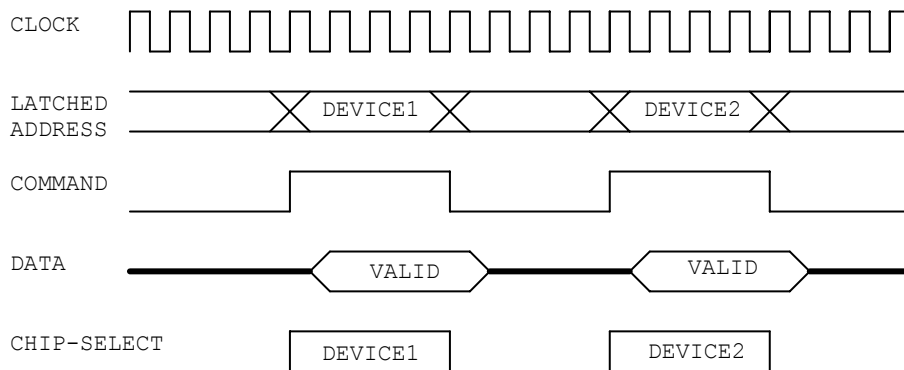
OPERATION

When a port or memory read instruction is executed by a CPU, its data pins first become tri-stated to receive data on the data bus, the CPU then puts out an address on the address bus and command signals on the command lines (/MR, /IR, /INTA, etc). An address decoder then decodes the address and command signals to form chip-selects for the target peripheral. The target peripheral then drives data on the bus using tri-state buffers, enabled with the chip-select input.

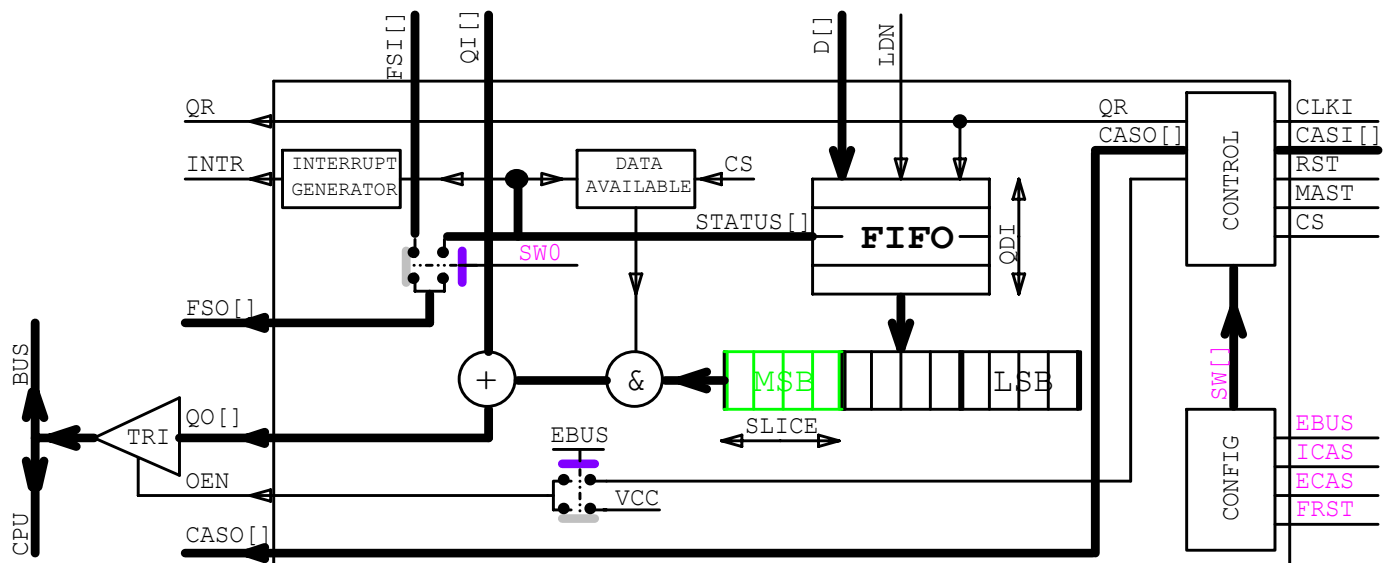
The DBIR component on the one hand takes away the chore of designing such an interface and on the other adds a number of resource saving and timing flexibility features.

The component takes the chip-select for the designated peripheral and shifts the data from the peripheral on the bus, synchronous to the system clock, at the start of the chip-select pulse. If the data width is larger than the bus width, the component disassembles the data into slices, shifting each slice onto the bus at the start of its respective chip-select.

BASIC READ CYCLE



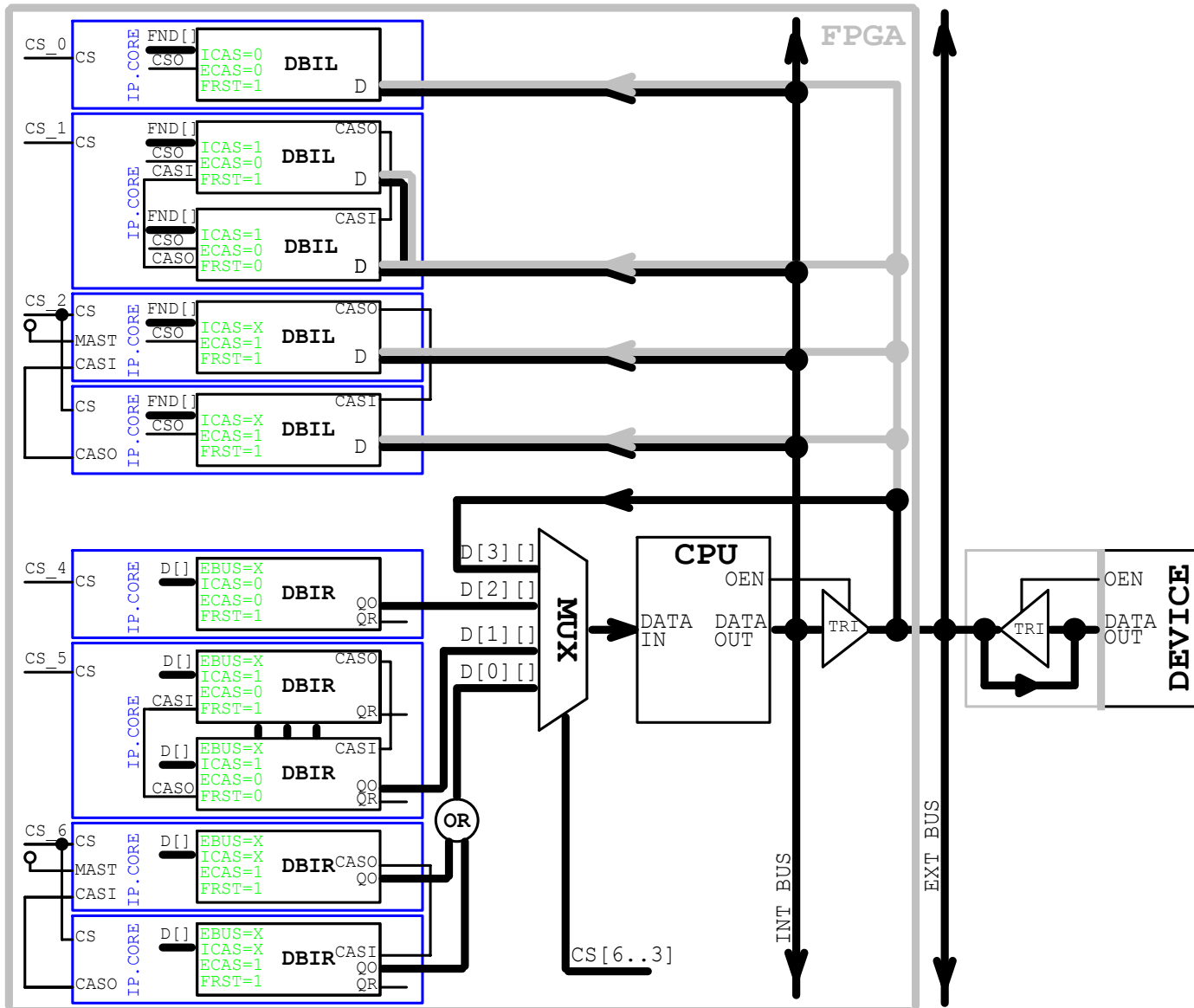
BLOCK DIAGRAM



CPU CONNECTION

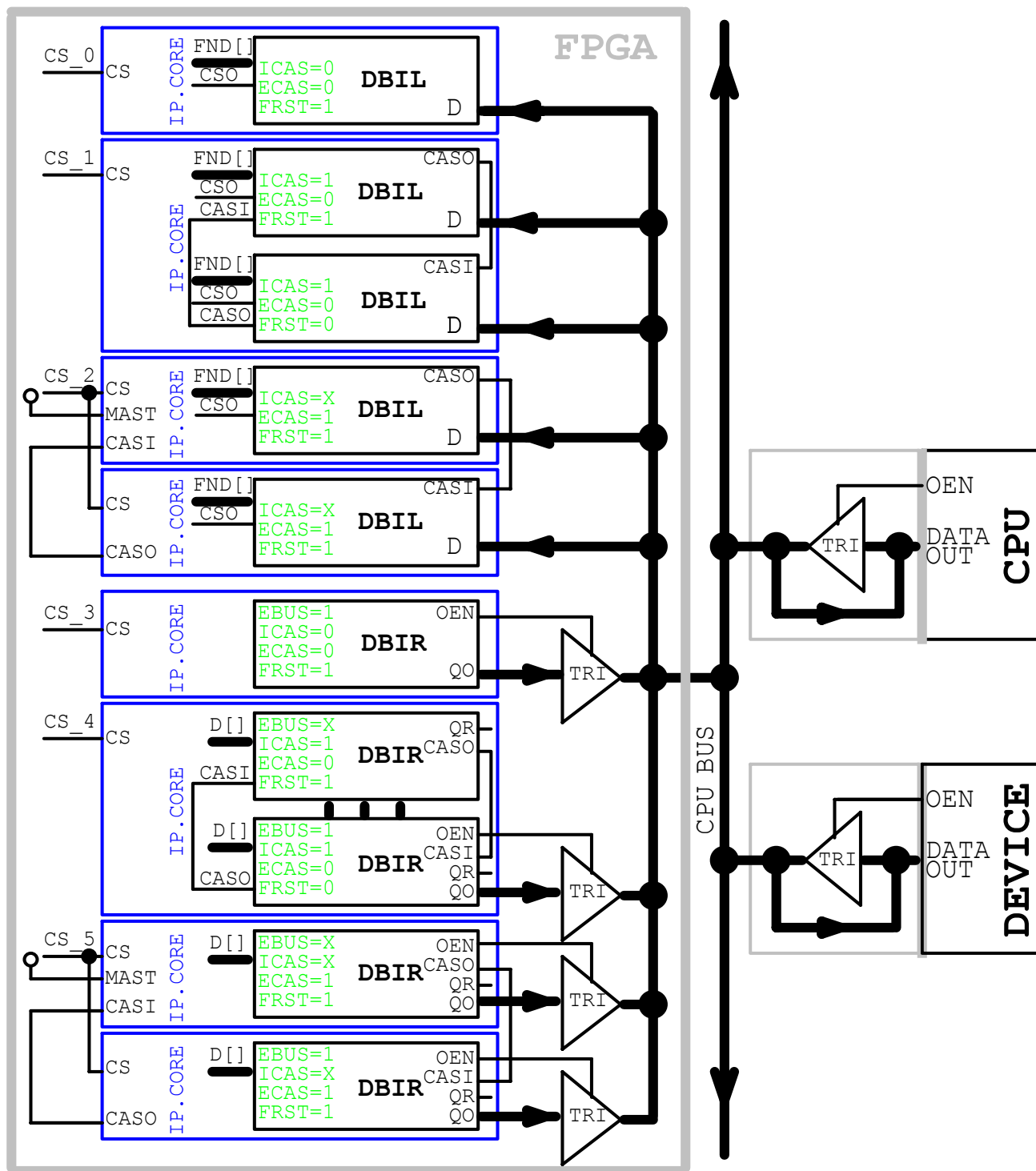
UNI-DIRECTIONAL CPU BUS

When a CPU has uni-directional buses for input and output data, as is often the case with CPUs and microcontrollers embedded in PLDs, the input data requires multiplexing. Output data from the CPU can be taken from either the internal or external (shown in grey) bus, with the internal bus being more advantageous. Since the external bus is bi-directional, it needs to be fed by tri-state buffers.



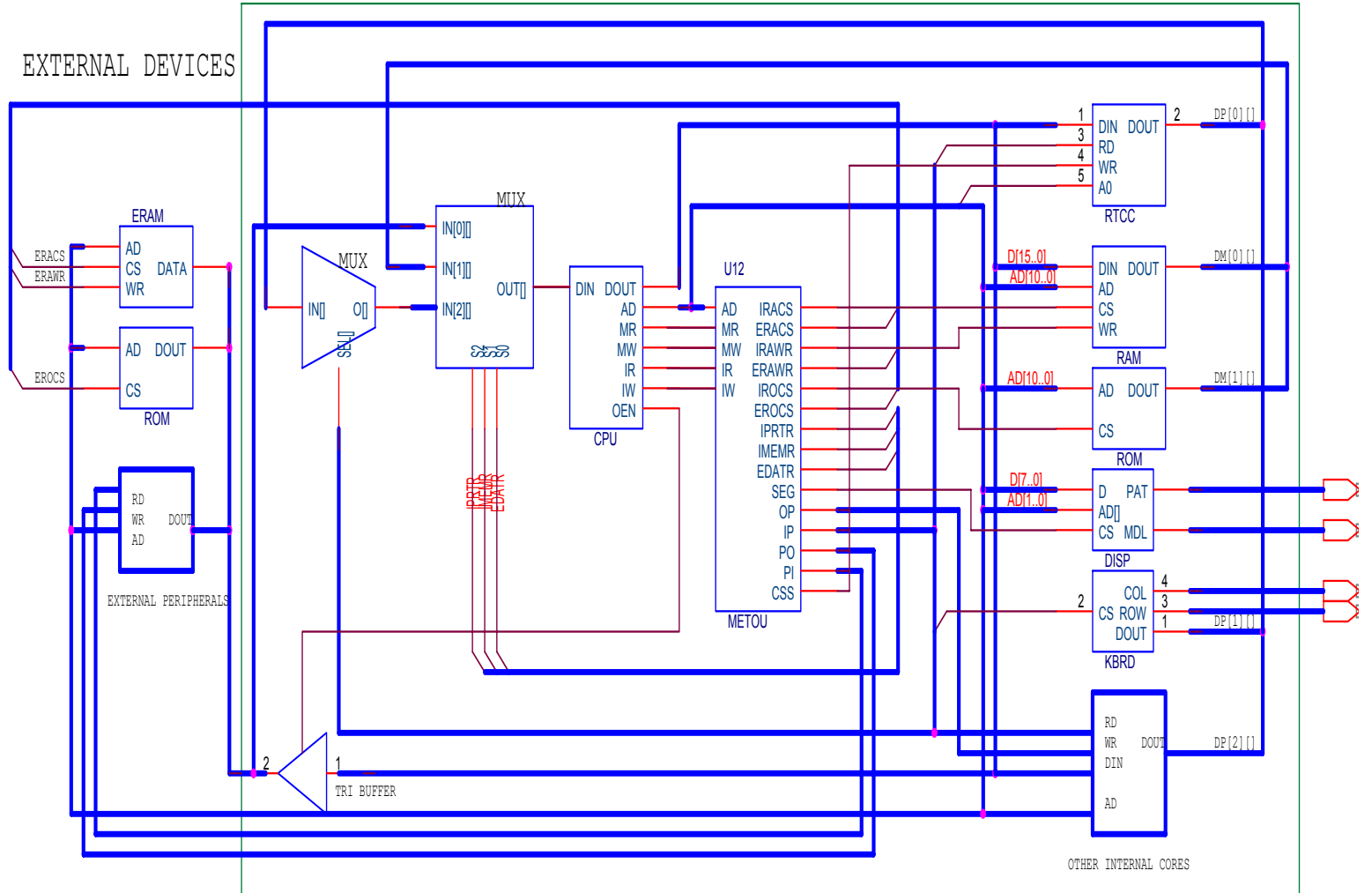
BI-DIRECTIONAL CPU BUS

When a CPU has a bi-directional bus for input and output data, as is often the case with discrete CPUs and microcontrollers, input and output data are taken from the external bus. Since the bus is bi-directional, it needs to be fed by tri-state buffers.



MICROPROCESSOR SYSTEM

FPGA



CASCADING

The DBIR component can be configured for various cascading options depending on the FRST, ECAS and ICAS parameters. Each of these options is described in detail below:-

Internal cascade chain not Externally cascaded

Formed of one or more DBIR components, with ECAS=0 and ICAS=1, linked end to end. The first component in the chain has FRST=1 and its MAST i/p unconnected. The CASO o/p of the last is fed back to the CASI i/p of the first.

The process starts after reset, with one of the DBIR components, known as the Master component, being enabled for data transmission. The selection of this component is made by setting its FRST parameter to '1' and is the first component in the chain.

The Master transmits its data word in slices, contiguously, with the MSB slice first. After the last slice, the next DBIR component is enabled. After the last component in the chain has completed its transmission, it pulses its CASO o/p, which being fed back to the Master Component, re-starts the process.

If the chain has only one component, its ICAS may be set to 0, in which case the component is automatically enabled after the last slice of the current data word transmission. The CASO F/B is optional.

Each component in the chain is fed with a common Chip Select (CS) and a unique data source. A combined o/p, to the CPU bus, is taken from the QO output of the last component in the chain.

External cascade chain

An internal chain that is not externally cascaded has one output node, to the CPU bus and one Chip Select. If the same Chip Select is required for data transmission from other designs (megafunctions/chips) each with their own connections to the CPU bus, then each design requires an internal chain.

The First DBIR component of one of these chains, needs to be selected as a Master to be enabled after reset. When only one internal chain was present, there was only one component with FRST=1. When multiple internal chains are present, a component with FRST=1, selected as the Master must have its MAST i/p is connected to VCC. This chain is then the Master Chain and the others, Slave Chains.

Each of the internal chains gives a single bus output, from its last component, thus an external chain has multiple outputs, one from each internal chain. All the chains are fed by a common Chip Select. The CASO o/p of the last Component of each chain is fed to the CASI i/p of the Master Component of the next chain. Thus the CASO o/p of the last component of the last chain, is fed to the CASI i/p of the Master Component of the Master Chain.

CHAIN CONFIGURATION

CMODE	PARAMETER		CHAIN CONFIGURATION
	ECAS	ICAS	
0	0	0	Internal Standalone, External Standalone
1	0	1	Internal Cascade , External Standalone
2	1	0	Internal Standalone, External Cascade
3	1	1	Internal Cascade , External Cascade

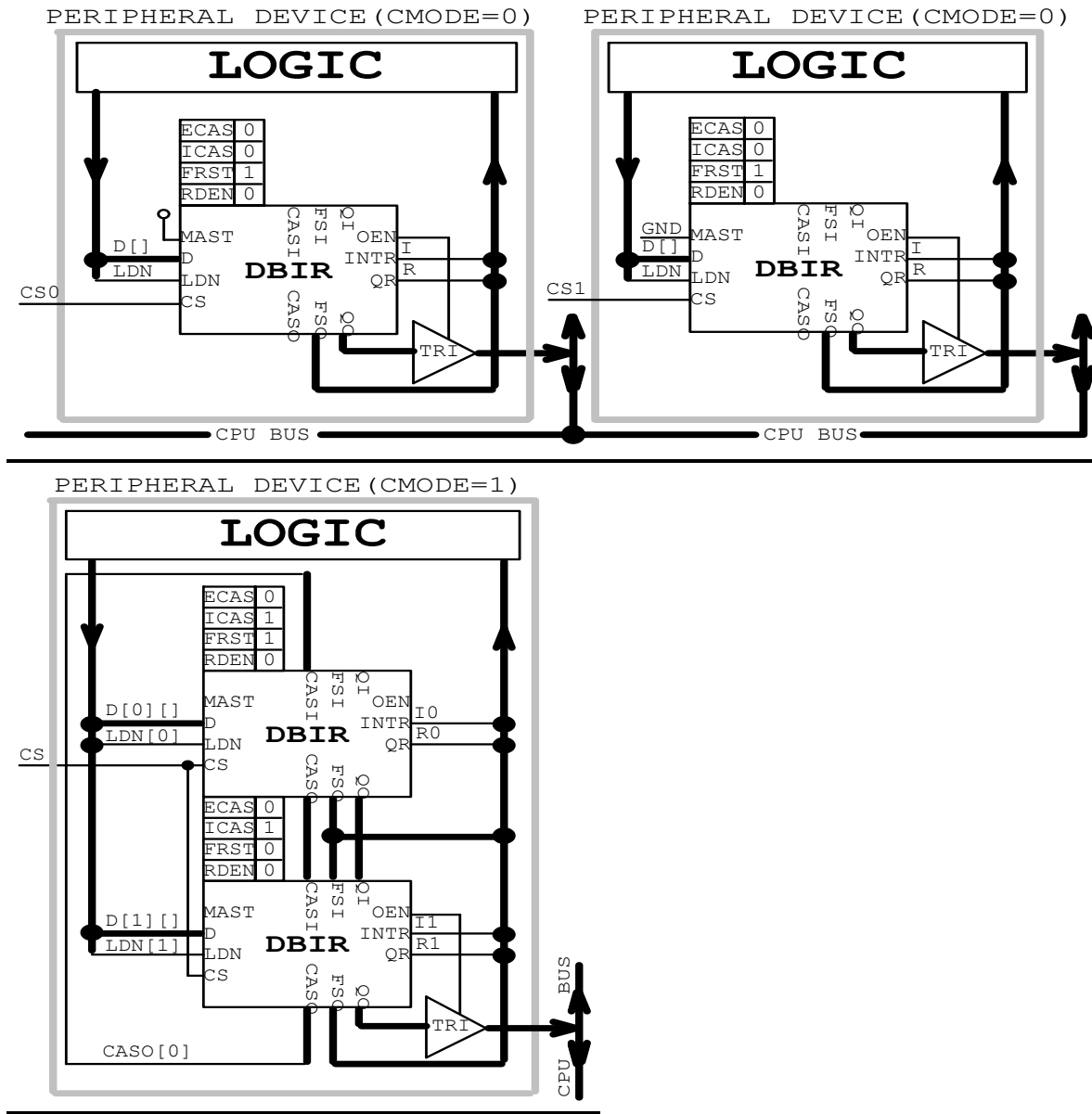
COMPONENT CONFIGURATION

PMODE	CMODE	PARAMETER	I/P	COMPONENT CONFIGURATION
		FRST	MAST	
0	0,2	0	NC	Disabled & bypassed
1	0	1	NC	Internal Standalone, External Standalone (Master Component)
2	1	0	NC	Internal Cascade , External Standalone (Slave Component)
3	1	1	NC	Internal Cascade , External Standalone (Master Component)
4	3	0	NC	Internal Cascade , External Cascade (Slave Component)
5	2,3	1	VCC	Internal Cascade , External Cascade (Master Component, Master Chain)
6	2,3	1	GND	Internal Cascade , External Cascade (Master Component, Slave Chain)

CASO, CASI CONNECTION

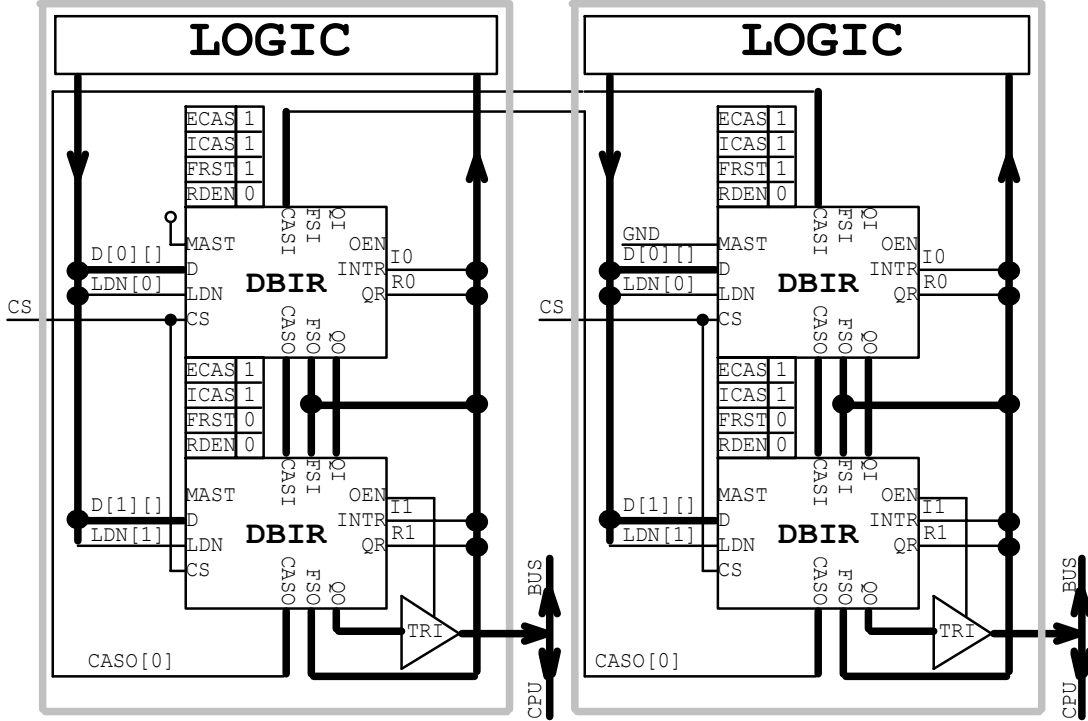
P.MODE	CASO and CASI connection	
0	CASO shorted internally to CASI	
1	CASO & CASI are unconnected .	
2	If last in the internal chain, Otherwise	connect CASO to CASI of Master , in same chain connect CASO to CASI of next , in same chain Connect CASI to CASO of previous , in same chain
3		Connect CASI to CASO of last , in same chain CASO to CASI of next , in same chain
4	If last in the internal chain, Otherwise	connect CASO to CASI of Master , in next chain connect CASO to CASI of next , in same chain Connect CASI to CASO of previous , in same chain
5,6	If last in the internal chain, Otherwise	connect CASO to CASI of Master , in next chain connect CASO to CASI of next , in same chain Connect CASI to CASO of last , in previous chain

CHAIN CONFIGURATION



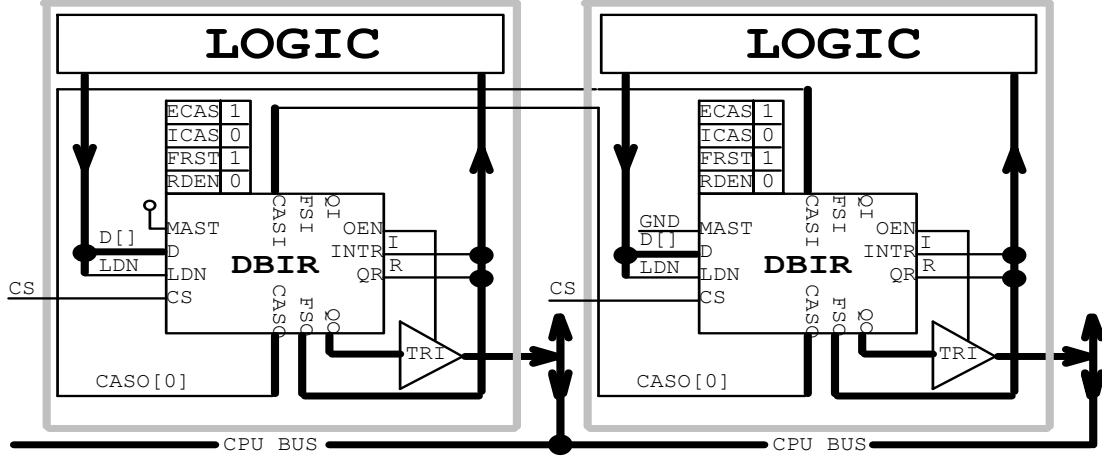
PERIPHERAL DEVICE (CMODE=3)

PERIPHERAL DEVICE (CMODE=3)

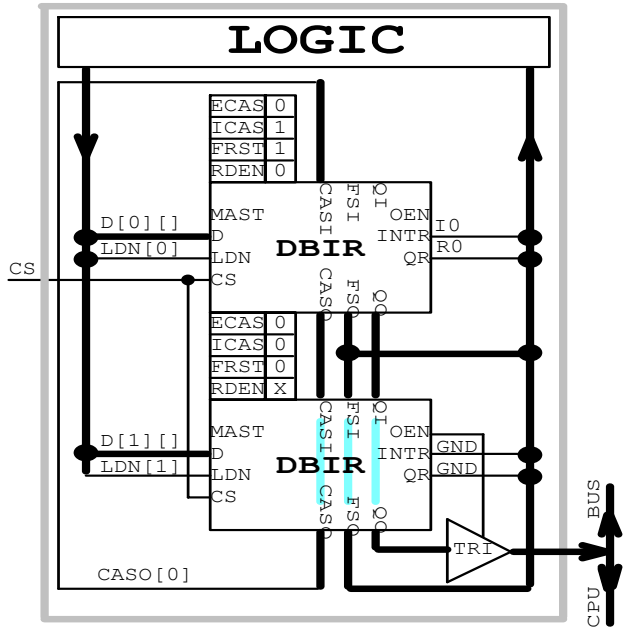


PERIPHERAL DEVICE (CMODE=2)

PERIPHERAL DEVICE (CMODE=2)



CHIP/MEGAFUNCTION



DISABLED COMPONENTS

When FRST+ICAS=0 a DBIR component is disabled and bypassed.

If the component is in an internal cascade chain, its OEN is the OEN of the previous DBIR. If it is standalone, its OEN output depends on its CASI input and drives low, if CASI is low.

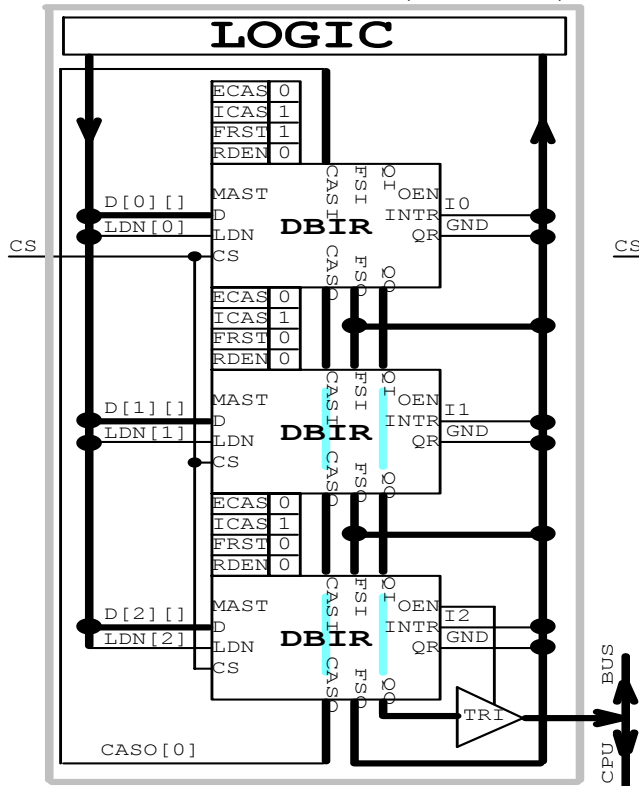
The QO, FSO and CASO outputs are shorted to the QI, FSI and CASI inputs.

The INTR and QR outputs drive low. The MAST, LDN, D[] and CS inputs are ignored.

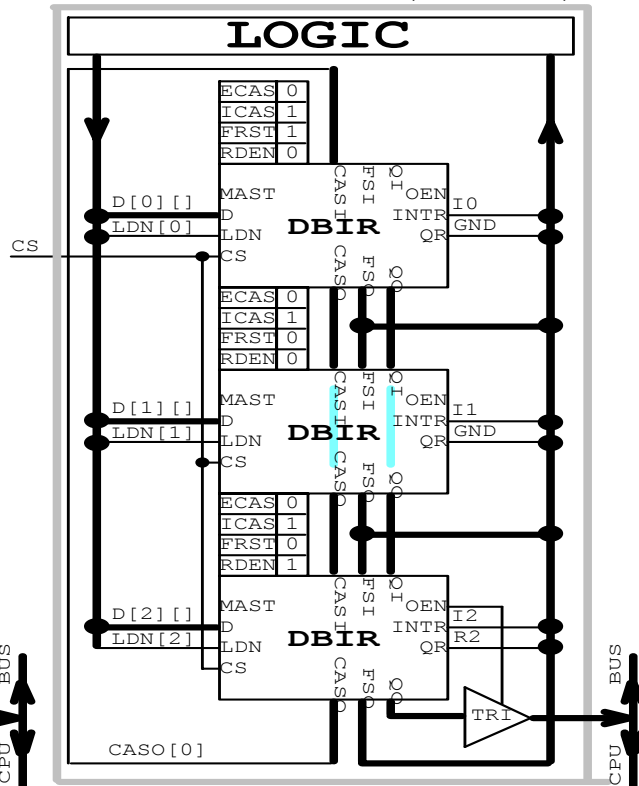
CHAIN HOPPING

A DBIR component read while data is not available (top left), it is an offending component and its QR O/P is low until available data is read. All subsequent DBIR components in the cascade chain are disabled, for all except load (LDN i/p) operations to their internal FIFO and external REG. The FSO and INTR O/Ps of the disabled components (left-bottom two) are available and the outputs (shown in green) are shorted to their I/Ps. These components are effectively removed from the cascade chain and the CS signal now reads only the offending component. If a disabled component, is to be kept enabled (bottom right), its RDEN parameter must be made 1.

PERIPHERAL DEVICE (CMODE=1)



PERIPHERAL DEVICE (CMODE=1)



NUMBER OF SLICES (N)

The width of each slice is the width of the data bus.
The data bus width need not divide the data width by an integer.

A Framing bit is required to be placed as the MSB bit indicating if the data read was valid. This bit is required, if I/P data is not always available ie when FRM=1.

```
IF QDE+QDI=0          --Depth of FIFO+Ext data register
  IVL=1              --I/P data always available since no buffering specified
ELSE
  IVL=IDV           --I/P data always available when IDV=1
END IF
N=(WSZ+1-IVL)/SWD   --Add 1 If remainder>0 and truncate to integer
```

Where:-

'N' is the number of slices of data sent to the CPU
'WDZ' is the bit width of the data to be sent to the CPU.
'SWD' is the bit width of a slice of data sent to the CPU.

EXAMPLE - For WSZ=7, SWD=3, IDV=0, QDI=1 and QDE=0:-

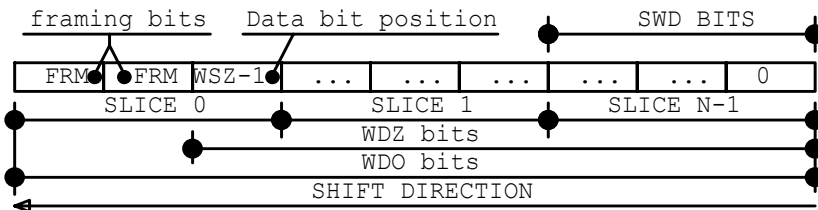
```
IVL =IDV          =0
N   =[7+1]/3     =2 rem 2   = 3
```

DATA STRUCTURE

When IVL=0, the bit positions labelled 'FRM' are '1', if the CPU reads unavailable data and '0', if it reads available data. When IVL=1, they are always '0'.

WDO=N*SWD --Width of the internal shift register

EXAMPLE - For N=3 and SWD=3 => WDO =9



BUFFERING

Internal buffering in the DBIR component depends on the SWD,WDZ,QDI and QDE parameters and consists of a Shift register and a FIFO buffer.

SHIFT REGISTER

The SWD and WDZ parameters determine the value of 'N', described above.
If **N>1**, a shift register is **used**. If **N=1**, a shift register is **not used**.

INTERNAL FIFO & EXTERNAL REGISTER

An internal FIFO, QDI words, WSZ bits wide. If input data 'D[]', comes from an external register loaded with LDN, then QDE is one. The internal FIFO and the external register are both loaded with LDN and the internal FIFO level status (FSO[]) includes a count for the external register(if QDE=1).

Overflow

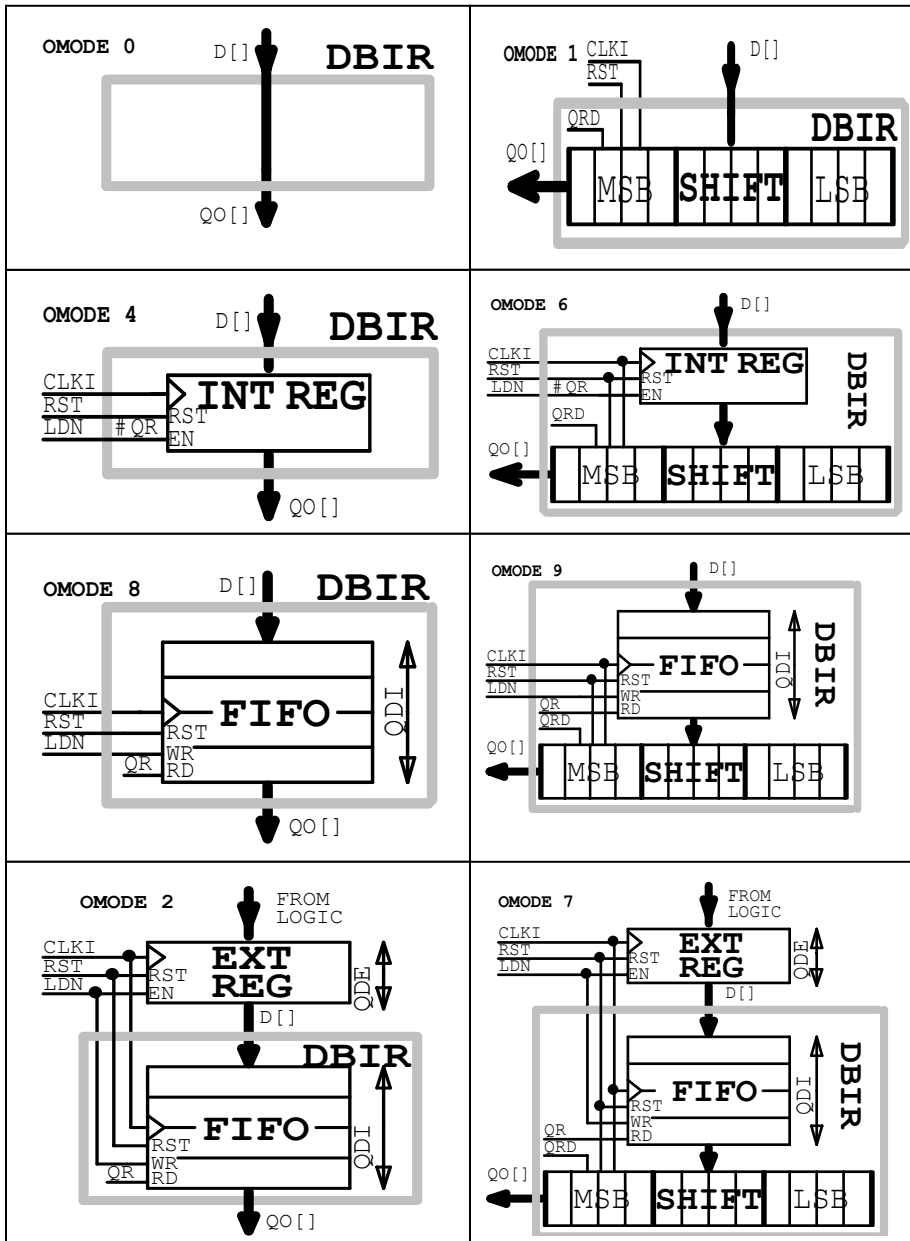
When IVL=1 - Cannot occur.
When IVL=0 - Safeguard not provided in the DBIR component. Overflow will cause level status (FSO[]) to rollover.

Underflow

When IVL=1 - Cannot occur.
When IVL=0 - The QR O/P, which causes the FIFO to deplete, doesn't appear if the FRM bits are '1', hence underflow can't occur.

OPERATION MODE

OMODE	OPERATION MODE				CS Hi CLKS (min)	CS Lo CLKS (min)	1st QO[] After RST	FRM bits Present
	SHIFT REG	Int FIFO	Ext REG	IVL				
0	No	No (QDI=0)	No (QDE=0)	1	1	1	Valid Data	No
4A/4B	No	Yes (QDI=1)	No (QDE=0)	1/0	1	1	Valid Data	No/Yes
8	No	Yes (QDI>1)	No (QDE=0)	0	1	1	All Hi, junk	Yes
2	No	Yes (QDI>=0)	Yes (QDE=1)	0	1	1	All Hi, junk	Yes
1	Yes	No (QDI=0)	No (QDE=0)	1	1	CLTL+2	All Hi, junk	No
6A/6B	Yes	Yes (QDI=1)	No (QDE=0)	1/0	1	CLTL+2	All Hi, junk	No/Yes
9	Yes	Yes (QDI>1)	No (QDE=0)	0	1	CLTL+2	All Hi, junk	Yes
7	Yes	Yes (QDI>=0)	Yes (QDE=1)	0	1	CLTL+2	All Hi, junk	Yes



INPUT PORTS

NAME	DESC	BITS	COMMENTS
D	Data->CPU	IWD	Data from a megafunction that needs to be sent to a CPU.
CLKI	Clock	1	Synchronizes all internal operations.
RST	Reset	1	Active Lo. Resets all internal registers.
LDN	Load FIFO	1	1 CLKI wide pulse. Active Hi. Loads FIFO & Ext register. Unused when QDI+QDE=0. (See 'Buffering'). At the falling edge of LDN If internal FIFO is not full, it is loaded with I/P data. If full, the external register (QDE>0) is overwritten. Level status(FSO) of the combined FIFO is incremented.
CS	Chip Select	1	Active Hi pulse. Common to all the components in a chain. Must be synchronous to the rising or falling edge of the CLKI input. See 'OPERATION MODE' for timing constraints and 'CASCADING' for information
MAST	Master	1	Component is master in Internal chain that is(1)/is not (0) master in an External chain.
QI	Cascade	BSW	Connect to QO output of previous component in a chain. Unused when FRST=1 or ICAS=0
FSI	Cascade	4	Connect to FSO output of previous component in a chain. Unused when FRST=1 or ICAS=0
CASI	Cascade	4	In 'Standalone' configuration it is unused, otherwise connected to CASO output of previous component in the chain. In the Master Component of a chain CASI[3..1] are unused. (See 'CASCADING')
COM	Reserved	1	No connect

OUTPUT PORTS

NAME	DESC	ACTIVE	BITS	COMMENTS
CASO	Cascade out	-	4	In a 'Standalone' configuration, it is unused, otherwise connected to the CASI i/p of the next component. (See CASI)
QO	Data Out	-	BSW	A data slice shifted out to the CPU. Use the output of the last component in an Internal chain and connect it to the input of a TRI-STATE buffer(EBUS=1), or to the input of a data mux(EBUS=0).
OEN	Output Enable	HI	1	Use output of the last component in an internal chain to enable TRI-STATE buffers connected to the QO[] output, when EBUS=1. When EBUS=0, it drives out Hi.
FSO	FIFO Status	-	4	Combined FIFO (see 'Buffering') level status. Counts 0 to QDI+QDE-1. Unused when QDI+QDE=0. FSO(0) ---- Almost empty (0 or 1 words left) FSO(1) ---- Full FSO(2) ---- Empty FSO(3) ---- Almost Full (0 or 1 spaces left)
INTR	Interrupt	HI	1	A one CLKI wide pulse after the LDN i/p, if FSO[1]=hi. Lo when FRST+ICAS=0.
QR	Data Load	HI	1	When available data is read(FRM bits are '0'), the QR pulse appears after the -ive edge of the CS, of the last slice. (See 'Data Structure', 'Buffering'). At the falling edge of QR, the FIFO including the external register(QDE=1) is depleted by 1 and the Level status(FSO) is decremented.

PARAMETERS-(All Integer type)

NAME	DESCRIPTION	COMMENTS
OPN	Memory/Register	FIFO options. See FIFO.DOC with
WR2	EAB Width option	QDE=QDE, QDI=QDI, WID=WSZ, WR2=WR2, DR2=DR2, OPN=OPN, DVC=DVC
DR2	EAB Depth option	
DVC	Device Family	
QDI	FIFO depth	Depth of internal FIFO. When IDV=1, QDI<=1-QDE. When IDV=0, no limit.
QDE	Registered I/P	I/P is registered with LDN as clock enable-Yes(1)/No(0)
IDV	Input Data Always Available	When IDV=1, input data is assumed to be always available. When IDV=0, the LDN signal writes data to the FIFO(QDI>0) and/or an external register(QDE=1). The DBIR component reads this data depending on the level count (FSO[]). If data is not available, a framing bit(MSB=1) is inserted.IDV is forced to 1, if QDI+QDE=0.
RDEN	Enable Component	To disable 'Chain Hopping' make RDEN=1, otherwise RDEN=0. Unused in a Master component and in a Slave, if the IDV parameter of the previous component is one.
EBUS	O/P Bus Type	Output data (QO[]) is taken from the DBIR component at the bottom of an internal cascade chain. The EBUS parameter of only this component is used and is set to '1', if the target data bus is bi-directional and '0' otherwise.
ICAS	Internal Cascade	Internal chain has one (0)/more than one(1) DBIR components. Component disabled when ICAS+FRST=0. See 'DISABLED', 'CASCADING'.
ECAS	External Cascade	Internal chain is(1)/is not (0) part of an External chain
FRST	First in chain	Component is the Master(1)/Slave(0) in the internal chain. Disabled when ICAS+FRST=0. See 'DISABLED', 'CASCADING'.
BSW	Width of QO[]	Width of Data bus and QO[] o/p. BSW>=1
SWD	Width of slice	MSBs beyond relevant data in QO[] are padded w/ '0'. The width of relevant data in QO is SWD with range 1<=SWD<=BSW. SWD _{MAX} limited internally to BSW. If SWD=0 it is forced to BSW
WSZ	Width of D[]	Width of D[] i/p, data from top hierarchy design to be sent to CPU. IWD>=WSZ>=1. WSZ _{MAX} limited internally to IWD.
IWD	Width of D[]	Relevant width of D[] i/p. 1<=IWD
CLTL	Shift Reg load Latency	When N>1, a shift register is used to shift data out, in slices. CLTL specifies the number of clocks, the rising edge of its load pulse is delayed, from the falling edge of the CS, of the last slice, allowing data to settle at the input of the register. CLTL>=1 (N>1), unused (N=1).See "Underflow" for CLTL and "Number of Slices" for N
EXC	Reserved	Must be 0, always

SAMPLE DESIGN (CMODE=3)

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
    PORT (
        D      :IN      BUS1D(NTI(WSZ) DOWNTO 0);
        CLKI   :IN      NODE:= '1';
        RST    :IN      NODE:= '1';
        CS     :IN      NODE:= '1';
        LDN    :IN      NODE:= '1';
        MAST   :IN      NODE:= '1';
        CASO   :BUFFER  NODE;
        QO     :BUFFER  BUS1D(BSW-1 DOWNTO 0);
        OEN    :BUFFER  NODE;
        EMPTY :BUFFER  NODE;
        INTR   :BUFFER  NODE;
        QR     :BUFFER  NODE
    );
END MYTOP;
ARCHITECTURE MYTOP OF MYTOP IS

    SIGNAL CASI :BUS1D(3 DOWNTO 0);

BEGIN
    CASI<="000" & CASO;

A1: D_BIR GENERIC MAP (TAKE FROM SIMULATION SECTION)
    PORT MAP (
        D      => D      , CLKI => CLKI, RST   => RST  , CS     => CS   ,
        LDN    => LDN   , MAST => MAST, CASI  => CASI , CASO(0) => CASO,
        QO     => QO   , OEN  => OEN , FSO(1) => EMPTY, INTR  => INTR,
        QR     => QR
    );
END MYTOP;
```

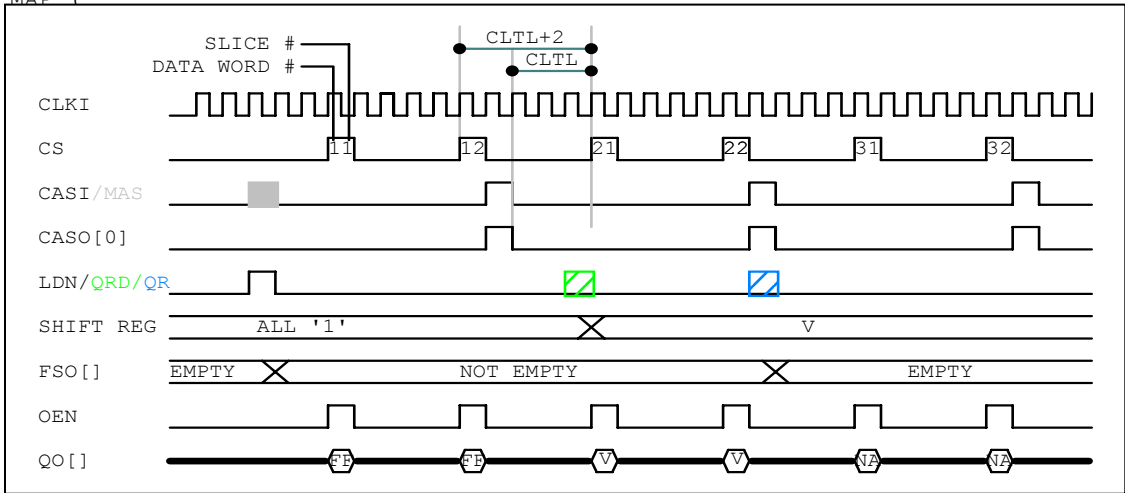
SAMPLE DESIGN-GENERIC STATEMENT & TIMING

OMODE=6B

A1:D_BIR GENERIC MAP (

```

IWD => 7,
WDZ => 7,
BSW => 4,
SWD => 4,
ECAS => 1,
ICAS => 1,
FRST => 1,
QDI => 1,
QDE => 0,
IDV => 0,
EBUS => 1,
CLTL => 2
    
```

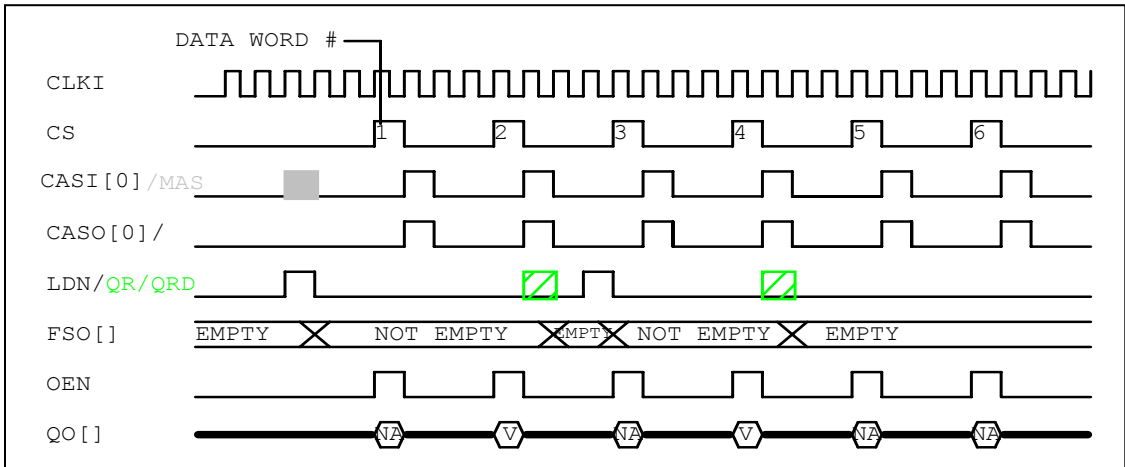


OMODE=4B

A1: D_BIR GENERIC MAP (

```

IWD => 7,
WDZ => 7,
BSW => 8,
SWD => 8,
ECAS => 1,
ICAS => 1,
FRST => 1,
QDI => 1,
QDE => 0,
IDV => 0,
EBUS => 1,
CLTL => 2
    
```

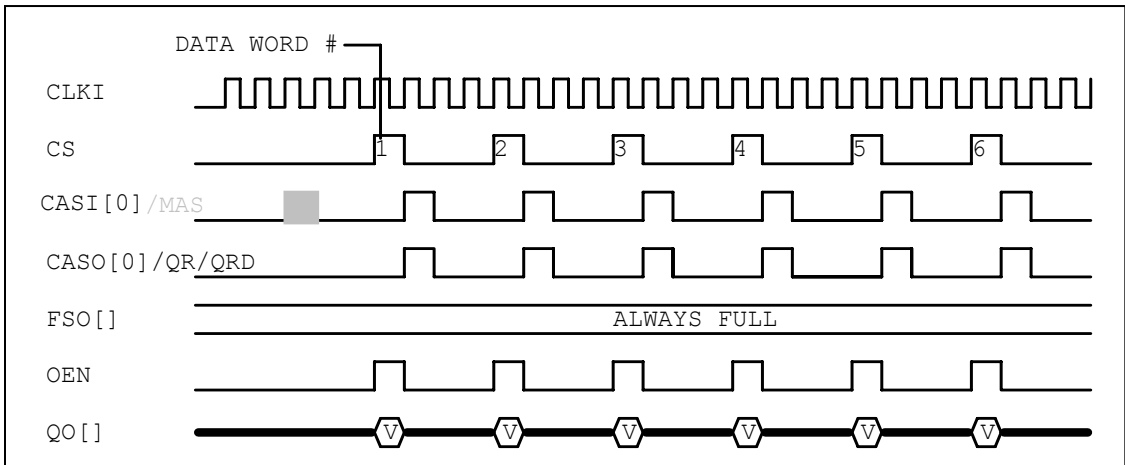


OMODE=0

A1: D_BIR GENERIC MAP (

```

IWD => 7,
WDZ => 7,
BSW => 8,
SWD => 8,
ECAS => 1,
ICAS => 1,
FRST => 1,
QDI => 0,
QDE => 0,
IDV => 0,
EBUS => 1,
CLTL => 2
    
```



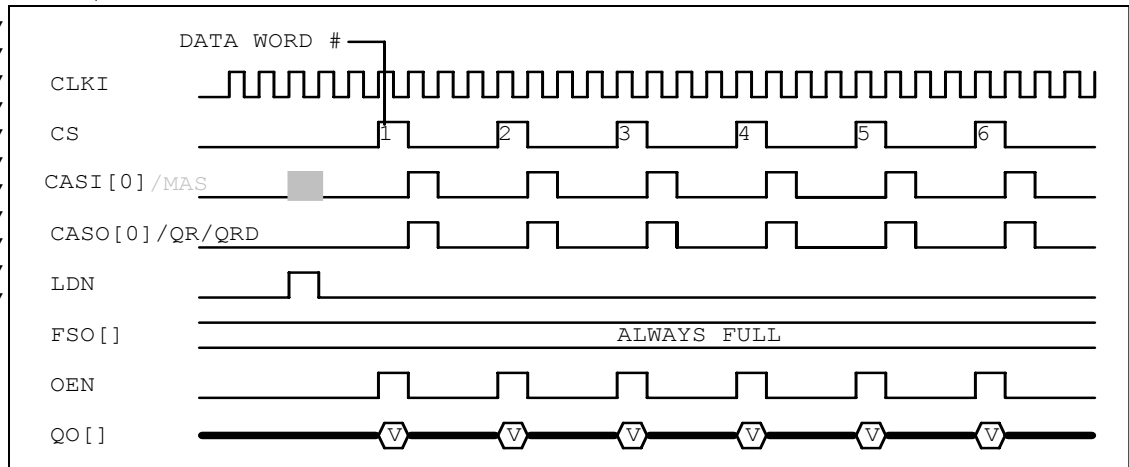
OMODE=4A

A1: D_BIR GENERIC MAP (

```

IWD => 7,
WDZ => 7,
BSW => 8,
SWD => 8,
ECAS => 1,
ICAS => 1,
FRST => 1,
QDI => 1,
QDE => 0,
IDV => 1,
EBUS => 1,
CLTL => 2
)

```



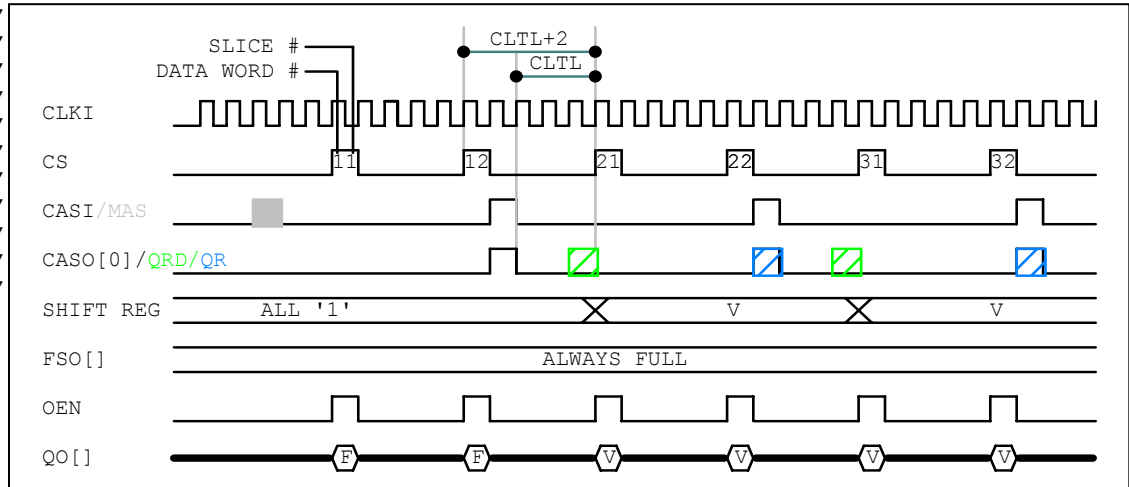
OMODE=1

A1: D_BIR GENERIC MAP (

```

IWD => 7,
WDZ => 7,
BSW => 4,
SWD => 4,
ECAS => 1,
ICAS => 1,
FRST => 1,
QDI => 0,
QDE => 0,
IDV => 0,
EBUS => 1,
CLTL => 2
)

```



OMODE=6A

A1: D_BIR GENERIC MAP (

```

IWD => 7,
WDZ => 7,
BSW => 4,
SWD => 4,
ECAS => 1,
ICAS => 1,
FRST => 1,
QDI => 1,
QDE => 0,
IDV => 1,
EBUS => 1,
CLTL => 2
)

```

