



CRC GENERATOR

DESCRIPTION

The C_RC.VHD ipcore described here is a serial LFSR (Linear Feedback Shift Register)

FEATURES

- User specified polynomial
- User specified Initial state
- Configurable register and input and output width.

APPLICATION

- Communication networks and ports such as: - USB, Ethernet, ATM, RS232, RS422, RS485 etc.
- A CRC is a linear feedback shift register (LFSR) with user defined polynomial use to encrypt data at transmission end and decrypt at receiver end. It is used to determine transmission errors.

VHDL Component Declaration:

```
COMPONENT C_RC
  GENERIC (INIZ      :INTEGER := 0;
          PLY       :BUS1D := "10001000000100001";
          WD        :INTEGER := 7;
          WQ        :INTEGER := 15
        );
  PORT (D           :IN  BUS1D(WD DOWNTO 0) := (OTHERS => '0');
        CLKI       :IN  NODE := '1';
        RST        :IN  NODE := '1';
        ENB        :IN  NODE := '1';
        LDN        :IN  NODE := '0';
        Q          :BUFFER BUS1D(WQ DOWNTO 0);
        DONE       :BUFFER NODE
      );
END COMPONENT;
```

FILES YOU GET

i) FUNC.DOC	-	Documentation of functions & data types used in the core.
ii) README.DOC	-	Compile and licensing information.
iii) CRC.DOC	-	This document
a) MYLIB.VHD	-	PACKAGE
b) C_RC.VHD	-	TOP HIERARCHY DESIGN FILE
c) R_SL.VHD	-	DESIGN FILE BELOW TOP HIERARCHY
d) S_DFF.VHD	-	-do-
e) F_DIV.VHD	-	-do-
f) U_DCNT.VHD	-	-do-
g) M_DFF.VHD	-	-do-
h) I_NCDEC.VHD	-	-do-
i) A_DSB.VHD	-	-do-
j) S_JKF.VHD	-	-do-
k) S_TFF.VHD	-	-do-
l) S_HIPT.VHD	-	-do-
m) P_AD.VHD	-	-do-



INPUT PORTS

Port Name	Required	Description	Comments
D	Yes	data input	WD+1 bits wide
CLKI	Yes	clock	Synchronizes all internal operations
RST	No	reset	Resets all internal registers
ENB	No	clock enable	-
LDN	Yes	data load	Active hi, 1CLKI wide (or more), loads D[] & starts process.

OUTPUT PORTS

Port Name	Description	Comments
Q	Result	WQ+1 bits wide.
DONE	Operation over	1 CLKI wide pulse after end of operation # clocks taken=WD+1

PARAMETERS

Parameter	Type	Required	Description
WD	INTEGER	Yes	Width of data (D[]), input port
WQ	INTEGER	Yes	Width of result (Q[]), output port
INIZ	INTEGER	Yes	Initial value of CRC-All 1's (0) or all 0's (1)
PLY	INTEGER	Yes	CRC polynomial. Polynomials conforming to any standard are supported. There is no restriction on the order of the polynomial.

SAMPLE DESIGN

```
-- Polynomial Equation      : X16 + X12 + X5 + 1
-- Conforming to standard  : X25 (SDLC, HDLC, CRC-CCITT)
```

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
```

```
LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;
```

```
ENTITY MYTOP IS
    PORT (CLKI    :IN  NODE;
          RST     :IN  NODE;
          D       :IN  BUS1D(7 DOWNT0 0);
          ENB     :IN  NODE;
          LDN     :IN  NODE;
          Q       :BUFFER BUS1D(15 DOWNT0 0);
          DONE    :BUFFER NODE
    );
END MYTOP;
```

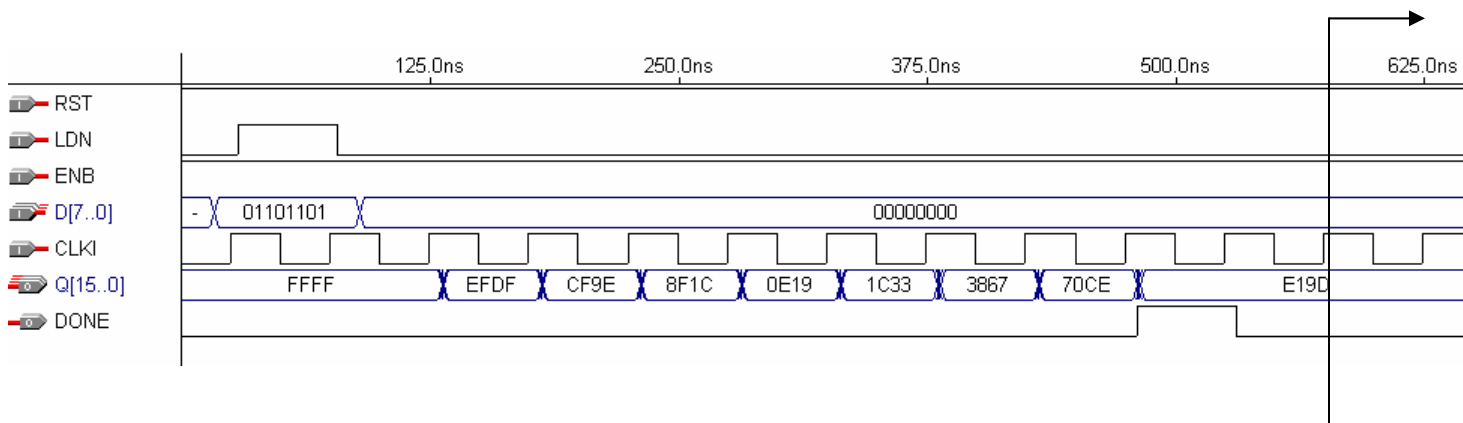
```
ARCHITECTURE MYTOP OF MYTOP IS
```

```
BEGIN
A1: C_RC GENERIC MAP (WD=>7, WQ=>15, INIZ=>0, PLY="10001000000100001")
    PORT MAP (D, CLKI, RST, ENB, LDN, Q, DONE);
END MYTOP;
```



TIMING DIAGRAM FOR SAMPLE DESIGN

Next LDN pulse



TIMING DIAGRAM – WD=7, WQ=15, INIZ=0, PLY="10001000000100001"

Next LDN pulse

