



ARRAY DIVIDER

DESCRIPTION

The A_DIV.VHD ipcore described here is a Array divider for signed or unsigned integer operands.

VHDL Component Declaration:

```
COMPONENT A_DIV
  GENERIC (
    DVWD : INTEGER;
    DSWD : INTEGER;
    QWD  : INTEGER;
    RWD  : INTEGER;
    SIG  : INTEGER
  );
  PORT (
    DVND : IN  BUS1D(DVWD-1 DOWNT0 0);
    DVSR : IN  BUS1D(DSWD-1 DOWNT0 0);
    QUOT : BUFFER BUS1D(QWD-1 DOWNT0 0);
    REMN : BUFFER BUS1D(RWD-1 DOWNT0 0)
  );
END COMPONENT;
```

FILES YOU GET

i) FUNC.DOC - Documentation of functions & data types used in the core.
ii) README.DOC - Compile and licensing information.
iii) ADIV.DOC - This document

a) MYLIB.VHD - PACKAGE
b) A_DIV.VHD - TOP HIERARCHY DESIGN FILE
c) P_AD.VHD - DESIGN FILE BELOW TOP HIERARCHY

INPUT PORTS

Name	Required	Description	Comments
DVND	Yes	Dividend	Signed/Unsigned integer DVWD bits wide
DVSR	Yes	Divisor	Signed/Unsigned integer DSWD bits wide

OUTPUT PORTS

Name	Required	Description	Comments
QUOT	Yes	Quotient	Signed/Unsigned integer QWD bits wide <u>QWD is normally = DVWD.</u> When $QWD < DVWD$, Quotient is truncated When $QWD > DVWD$, Quotient is padded with 0's(SIG=0), or sign extended(SIG=1).
REMN	No	Remainder	Unsigned integer RWD bits wide <u>RWD is normally = DVWD-SIG.</u> When $RWD < DVWD-SIG$, Remainder is truncated When $RWD > DVWD-SIG$, Remainder is padded with 0's.

PARAMETERS

Parameter	Type	Required	Description
DVWD	INTEGER	Yes	Width of dividend, input port
DSWD	INTEGER	Yes	Width of divisor, input port
QWD	INTEGER	Yes	Width of quotient, output port
RWD	INTEGER	Yes	Width of remainder, output port
SIG	INTEGER	No	Inputs are in signed 2's compliment format (1) or unsigned (0)



SAMPLE DESIGN

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY MYLIB;
USE MYLIB.MYLIB.ALL;

ENTITY MYTOP IS
    PORT(CLKI      :IN  NODE;
         DVND      :IN  BUS1D(10 DOWNT0 0);
         DVDR      :IN  BUS1D(12 DOWNT0 0);
         QUOT      :BUFFER BUS1D(23 DOWNT0 0)
    );
END MYTOP;

ARCHITECTURE MYTOP OF MYTOP IS
BEGIN

A1: A_DIV GENERIC MAP (DVWD=>11,DSWD=>13,QWD=>24,RWD=>0)
    PORT MAP (DVND,DVDR,QUOT);
END MYTOP;
```