VLSI DESIGN OF PARALLEL A to D INTERFACE CONTROLLER

An important feature in most embedded systems is the ability to acquire analog signals from the external world. Such signals require an A to D converter, for conversion to digital, in order to be read by a processor.

The A_DCC.VHD IP core, described here, is a parallel A to D interface controller and can be implemented as a descrete device in an FPGA/CPLD or ASIC.

This core provides all the necessary interface logic for a variety of parallel converters. An internal FIFO buffer, maximizes throughput and may be implemented in registers or memory. Automatic conversion keeps the internal FIFO buffer filled at all times, freeing embedded software of conversion control tasks. TRI-STATE outputs permit implementation as a discrete device on an external data bus. Flexible bus width permits interface with a variety of processors. Can be cascaded with other peripherals or used stand-alone. Any number of analog inputs, multiplexers and digital resolution allow for its use in large or small control applications. Flexible analog MUX settling time, eliminates cross-talk between channels. Bit filtering of the converter STATUS line ensures reliable operation. Interfaces with the processor on a single I/O read port. Synchronous design using a single global clock, ensures reliable operation over a range of clock frequencies and temperature.

FEATURES

- **Double buffered interface logic** allows configuration to **any bus width,** from **serial** to **parallel** of any width.
- Interface on data bus or port, **dedicated or shared.**
- Instantiate the core as **stand-alone** or **cascaded**, in a daisy chain configuration.
- **Daisy chain** multiple **cores** on **one port address**.
- Any number of **Analog inputs**.
- Any number of **Analog Multiplexers**.
- Any number of Bits of **resolution**
- **FIFO** buffer of **any depth** provided for maximum throughput
- **FIFO** may be implemented in **memory** or **registers**
- **Interrupt** CPU on **FIFO** full.
- Rising and falling edge **debouncing** of converter STATUS line with configurable **debounce interval**
- **TRI-STATE** outputs for implementation as a **descrete device ASIC** or **PLD.**
- **Interface** with CPU on a **single I/O read port.**
- Flexible MUX **settling time**, eliminates **cross-talk** between channels.
- **Automatic conversion** and **channel # rollover** allow continuous conversion without user intervention.
- **Any clock frequency**

APPLICATION

- Acquisition of analog data-pH, pressure, temperature, gas, voltage, current, flow rate etc.
- Industrial/Commercial control applications- Motor (AC/DC), Power (AC/DC), Robotics, Data-Loggers, Osciloscopes, Spectrum and logic analysers, DVMs, Power Meters, etc.

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VHDL Component Declaration:

```
COMPONENT A_DCC
      GENERIC (
            OPN   :INTEGER := 1;
            WR2   :INTEGER := 2;
            DR2   :INTEGER := 2;
            DVC   :INTEGER := 2;
            CASC  :INTEGER := 1;
            CHW   :INTEGER := 3;
            DBW   :INTEGER := 8;
            MAXC  :INTEGER := 2;
            CHPM  :INTEGER := 4;
            A_DC  :INTEGER := 1;
            LCH   :INTEGER := 8;
            STM   :INTEGER := 1;
            ADQ   :INTEGER := 0;
            CHQ   :INTEGER := 0;
            RCW   :INTEGER := 0;
            WD    :INTEGER := 16;
            DCN   :INTEGER := 1;
            EBUS  :INTEGER := 0
      );
      PORT(
            MAST  :IN   NODE;
            CASI  :IN   NODE;
            CLKI  :IN   NODE;
            RST   :IN   NODE;
            DIN   :IN   BUS1D(WD-1 DOWNTO 0);
            CS    :IN   NODE;
            STS   :IN   NODE;
            CASO  :BUFFER NODE;
            DOUT  :BUFFER BUS1D(DBW-1 DOWNTO 0);
            R_C   :BUFFER NODE;
            MXS   :BUFFER BUS1D(MAXC-1 DOWNTO 0);
            CNO   :BUFFER BUS1D(CHW-1 DOWNTO 0);
            INTR  :BUFFER NODE
      );
END COMPONENT;
```

FILES YOU GET

```
  i)FUNC.DOC   - Documentation of functions & data types used in the core.
 ii)README.DOC - Compile and licensing information.
iii)ADC.DOC    - This document

MYLIB.VHD      - PACKAGE
A_DCC.VHD      - TOP HIERARCHY DESIGN FILE
M_DFF.VHD      - DESIGN FILE BELOW TOP HIERARCHY
S_DFF.VHD      -          -DO-
P_AD.VHD       -          -DO-
P_DV.VHD       -          -DO-
D_ECOD.VHD     -          -DO-
U_DCNT.VHD     -          -DO-
A_DSB.VHD      -          -DO-
D_BIR.VHD      -          -DO-
S_TFF.VHD      -          -DO-
S_JKF.VHD      -          -DO-
```

DESIGN FILES BELOW TOP HIERARCHY

```
F_DIV.VHD      -         -DO-
B_SHIFT.VHD    -         -DO-
I_NCDEC.VHD    -         -DO-
P_LSE.VHD      -         -DO-
F_IFO.VHD      -         -DO-
M_TRI.VHD      -         -DO-
T_RI.VHD       -         -DO-
R_STK.VHD      -         -DO-
M STK          -         -DO-
```


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INTERFACE INFORMATION

The schemes described provide information on interfacing the core with other peripherals on a common data bus & ports. The two types of interface schemes described are:-

1) **Stand-alone** (bus or port)
2) **Cascaded** (bus or port)

In both the interface schemes the data bus and port can be of any size and can be shared with any number of peripherals. The Chip Select line (CS) must be unique for every core in the stand-alone scheme and common to all cascaded cores in the cascaded scheme. Chip-select signals can be generated either by an i/o address decoder, within the PLD(in the bus interface schemes) or from an output port on a micro-controller(in the port interface schemes).

Data from this core is sent out while the CS input is active. When EBUS=1, data must be routed through TRI-STATE buffers onto a bidirectional bus or port with the OEN output being used as the buffer enable. When EBUS=0, data from this core must be ORed with other cascaded cores and routed to a unidirectional input port with the common CS being used as a port enable (or as a mux select).

CASCADED

Set the CASC parameter to one and connecting the MAST input of the first core in the chain to logic 1. The CASO output of each core is connected to the CASI input of the next core in the chain and the CASO output of the last core in the chain to the CASI input of the master, or the first core in the chain.

In this scheme, cores must be accessed sequentially one after the other and the entire sequence must be completed everytime, in a process known as daisy chaining. The core, configured as the master transmits first, after RST, followed by the next core in the chain. After a core transmits its data, it pulses the CASO output and enables the next core in the chain, for transmission.

STAND-ALONE

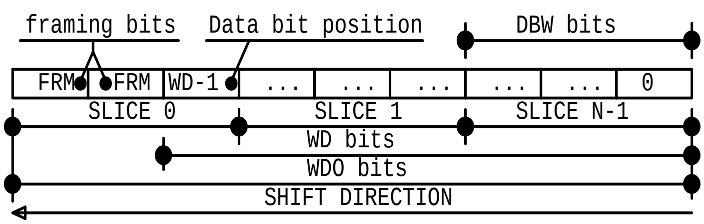
Set the CASC parameter to zero. MAST and CASI inputs are not used. The core is ready to transmit data after RST hi. The core with an active CS signal will send data . Separate chip selects for each core allow random access.

DATA READ

The number of bits of data sent to the CPU at a time depends on the number of data lines connected to the core. If the number of data lines connected is less than required a full word of data, data is sliced to the size of the data lines and must be read contiguously (MSB first) until the whole data word is assembled by the CPU. Analog data is read first and then, if CHQ=1, the channel number. When CHQ=1, the channel number is sent only after valid analog data, until then, invalid analog data is sent.

ANALOG DATA

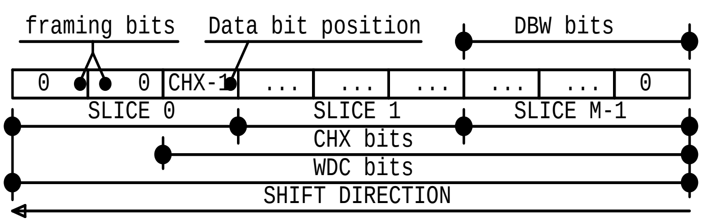
When DBW>WD , data is not sliced. The FRM bits indicate data validity->‘1’ for invalid data and ‘0’ for valid.
When DBW<=WD, data is sent in 'N' slices. The calculation of 'N' is shown below.



N=INT(WD/DBW) (if remainder present, add 1)
WDO=N*DBW

CHANNEL # DATA

When CHX<=DBW, data is not sliced and a valid channel # is sent whole on the bus.
When CHX>DBW, data is sent in 'M' slices. Framing bits, if any, are always 0.



CHX=1+Log2(LCH-1)
M=INT(CHX/DBW) (if remainder present, add 1)
WDC=M*DBW

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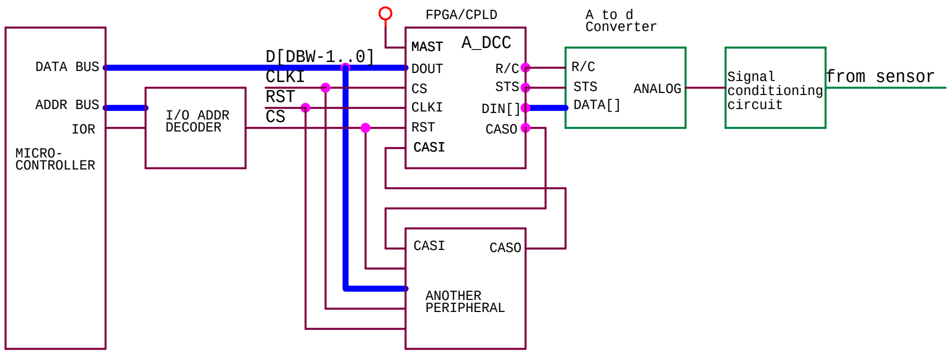
CIRCUIT DIAGRAMS

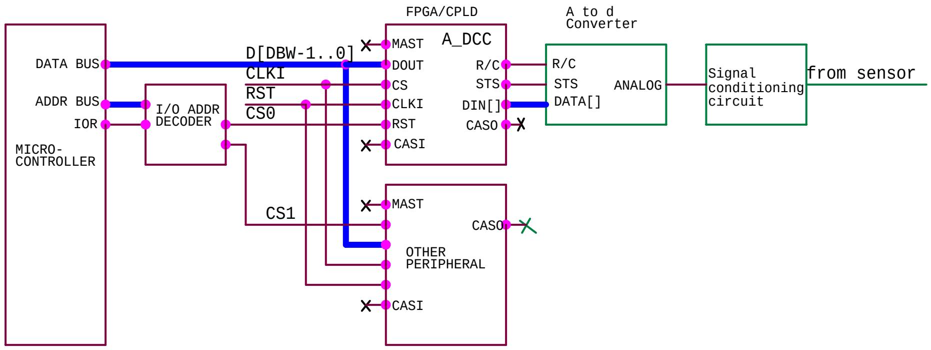
CASCADED BIDIRECTIONAL DATA BUS

Parameter CASC=1, EBUS=1



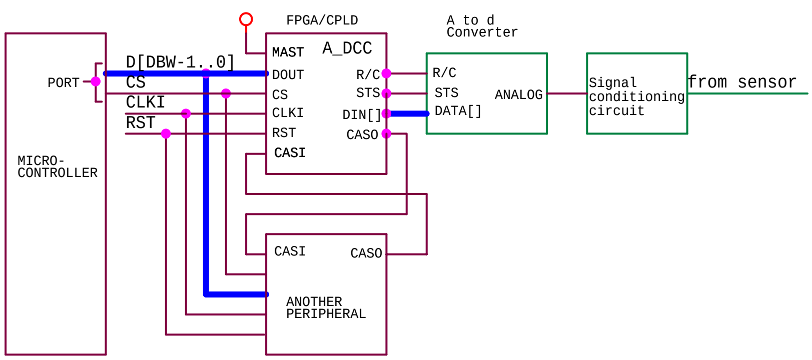
STAND-ALONE BIDIRECTIONAL DATA BUS

Parameter CASC=0, EBUS=1



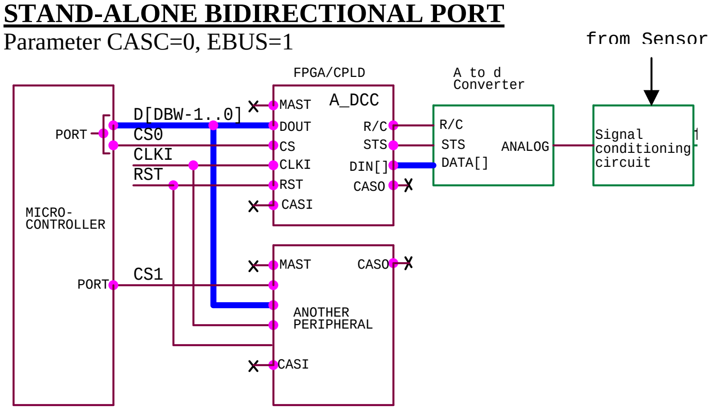
CASCADED BIDIRECTIONAL PORT

Parameter CASC=1, EBUS=1

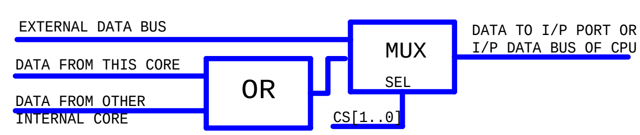


STAND-ALONE BIDIRECTIONAL PORT

Parameter CASC=0, EBUS=1



CONNECTION TO UNIDIRECTIONAL BUSES & PORTS (EBUS=0)



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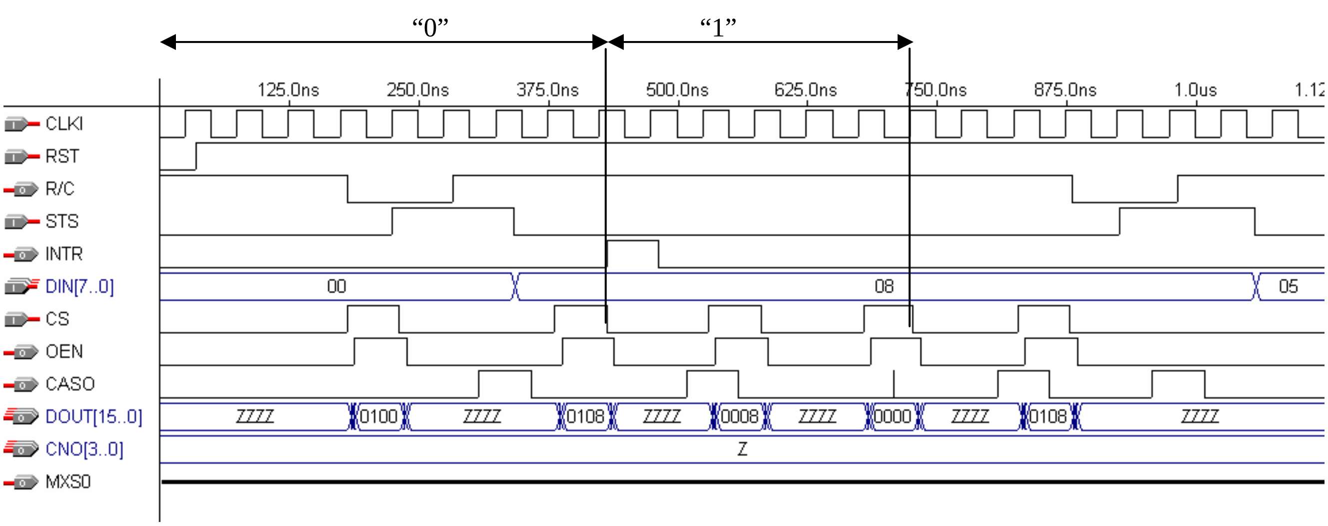
SAMPLE DESIGN-1

```
LIBRARY  IEEE;
USE  IEEE.STD_LOGIC_1164.ALL;
USE  IEEE.STD_LOGIC_ARITH.ALL;
USE  IEEE.STD_LOGIC_UNSIGNED.ALL;

LIBRARY  MYLIB;
USE  MYLIB.MYLIB.ALL;

ENTITY  MYTOP  IS
 PORT(MAST   :IN     NODE;
      CASI   :IN     NODE;
      CLKI   :IN     NODE;
      RST    :IN     NODE;
      DIN    :IN     BUS1D(7 DOWNTO 0);
      CS     :IN     NODE;
      STS    :IN     NODE;
      CASO   :BUFFER NODE;
      DOUT   :BUFFER BUS1D(15 DOWNTO 0);
      R_C    :BUFFER NODE;
      MXS    :BUFFER BUS1D(0 DOWNTO 0);
      CNO    :BUFFER BUS1D(2 DOWNTO 0);
      INTR   :BUFFER NODE;
 );
END  MYTOP;

ARCHITECTURE   MYTOP  OF  MYTOP  IS

BEGIN
A1: A_DCC GENERIC MAP(OPN=>0,CASC=>0,CHW=>4,DBW=>16,MAXC=>1,CHPM=>8,A_DC=>1,
                      LCH=>1,STM=>1,ADQ=>0,CHQ=>1,RCW=>0,=>WD=>8,DCN=>0,EBUS=>1)
          PORT    MAP('0','0',CLKI,RST,DIN,CS,STS,CASO,DOUT,R_C,MXS,CNO,INTR);
END  MYTOP;
```

SAMPLE DESIGN TIMING DIAGRAMS

1)Fifo empty, read invalid data - (section “0” in timing diagram)
2)Fifo full, interrupt CPU, read valid data and channel # - (section “1” in timing diagram)



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PARAMETERS AND PORTS

INPUT PORTS(All Widths are 1)

NAME	DESCRIPTION	COMMENTS
MAST	Master select	In a cascaded configuration(CASC=1), if core is a master, set to Hi else Lo. In a stand-alone configuration(CASC=0), it is unused.
CASI	Cascade in	In a cascaded configuration(CASC=1) , if core is not a master, connect to CASO of the previous core in the chain, if it is the master, connect to CASO of the last core in the chain. In a stand-alone configuration(CASC=0) it is unused and may be left open.
CLKI	Clock	Positive edge triggered. Synchronizes all internal operations
RST	Reset	Asynchronous, active lo, resets all internal logic
CS	Chip select	Active hi, enables data read logic. Must be synchronous to the CLKI input. Data appears on the 'DOUT' port while CS is hi. **TIMING**(See 'INTERFACE INFORMATION' for N & M) Hi time >=1 CLKI Lo time >=3 CLKI (M>1 or N>1) Lo time >=1 CLKI (M=1 and N=1)
STS	Converter Status	Status signal from A to D converter. When Hi, indicates conversion in progress. When Lo indicates data available.

OUTPUT PORTS

NAME	DESCRIPTION	WIDTH	COMMENTS
DOUT	Data bus	DBW	Bus containing analog to digital converted data. When EBUS=1, this bus is fed by TRI-STATE buffers, enabled while CS i/p is Hi. When EBUS=0, it is ANDed with CS, without TRI buffers.
R/C	Column	1	Read/Convert command to A to D. Read (Hi) / Convert (Lo)
CASO	Cascade out	1	Used in a cascaded configuration (CASC=1), to enable the next core in the chain for reading the bus. In a stand-alone configuration, it is unused & drives Lo. See CASI
MXS	MUX select	MAXC	Active Lo, analog mux select lines.
CNO	Channel #	CHW	Channel # lines, connected to analog mux
INTR	Interrupt	1	Interrupt pulse, 1 CLKI wide, on FIFO full.

PARAMETERS-all INTEGER type, Minimum value=0

NAME	DESCRIPTION
OPN WR2 DR2 DVC	There are two FIFO buffers, one for ADC data and one for channel number. See FIFO.doc with :- **For ADC data** QDE=1, QDI=ADQ, WID=WD, WR2=WR2, DR2=DR2, OPN=OPN, DVC=DVC **For CHANNEL # (if CHQ=1)** QDE=0, QDI=ADQ+1, WID=log2(LCH-1)+1, WR2=0, DR2=0, OPN=0, DVC=DVC
CASC	Cascaded/Standalone –1/0. Determines behaviour of MAST & CASI inputs and the CASO o/p.
CHW	Width of CNO[] output port
DBW	Width of DOUT[] and DIN[] ports. See "INTERFACE INFORMATION" above
MAXC	Number of analog muxes. MAXC>=LCH/CHPM. If result has remainder, add 1
CHPM	Number of analog channels per mux
A_DC	Reserved. Leave 1 or unused
LCH	Number of analog channels used. LCH<=CHPM*MAXC
STM	Number of CLKI pulses for Settling time, after channel # output to R/C Lo
ADQ	Word depth of internal FIFO
CHQ	Channel # is read by CPU ? - Yes/No – 1/0
RCW	Lo time width of R/C output. When RCW=0, R/C remains low until conversion starts, then goes Hi
WD	Bit width of analog data after conversion to digital
DCN	Debounce count for STS input (0-for no debounce)
EBUS	DOUT[] connected to bidirectional bus/port(1) or unidirectional bux/port(0)

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